Title	Page
Cover Sheet	1
Block Diagram	2
CPU-CLK/Control/MISC/PEG ,CPU-Memory	3,4
CPU-Power,CPU-GND	5,6
DDRIII DIMMA1&DDRIII DIMMB1	7,8
LYNX-PCI/E/DMI/USB/CLK	9
LYNX-SATA/HOST/FAN/GPIO/VGA	10
LYNX-SMB/LPC/AUDIO/RTC/RST	11
LYNX-POWER PIN,GND/ LYNX STRAPS	12,13 ,14
PCIE(X1) & PCIE(X16) Slots	15
SIO-NUVOTON NCT5533D	16
ALC887/VT1708S CE-Type C	17
LAN RTL8111G/8106E	18
SATA /Front USB3.0 Connector	19
USB3.0 Hub-VL805/UPD720201	20
Rear USB3.0 Connector	21
USB2.0 Connector	22
DVI	23
HDMI	24
VGA	25
ACPI Controller UPI	26
CPU Power - ISL95812	27,28
DDR Power -UP1504 1-Phase	29
PCH Power - OP+MOS	30
ATX F_Panel/EMI/TPM/LPT	31
Manual Parts	32

MS-7817 mATX Ver:30

Intel Sharkbay plamform H81

CPU:

INTEL-Haswell LGA1150

System Chipset:

H81

Memory:

DDRIII (1333/1666MHz) * 2 (Dual Channel)

PWM:

VRD12 - ISL95812

OnBoard Chipset:

HD Audio Codec:ALC887

LAN-realtek8111G

SIO:NUVOTON 5533D

SPI ROM: 64 MB

Other:

DVI*1
VGA*1
HDMI*1
SATA3*4
FRONT USB2.0 *4
FRONT USB3.0 *2
REAL USB2.0 *2
REAL USB3.0 *4

Expansion Slots:

PCI Express (X16) Slot * 1
PCI Express (X1) Slot * 2

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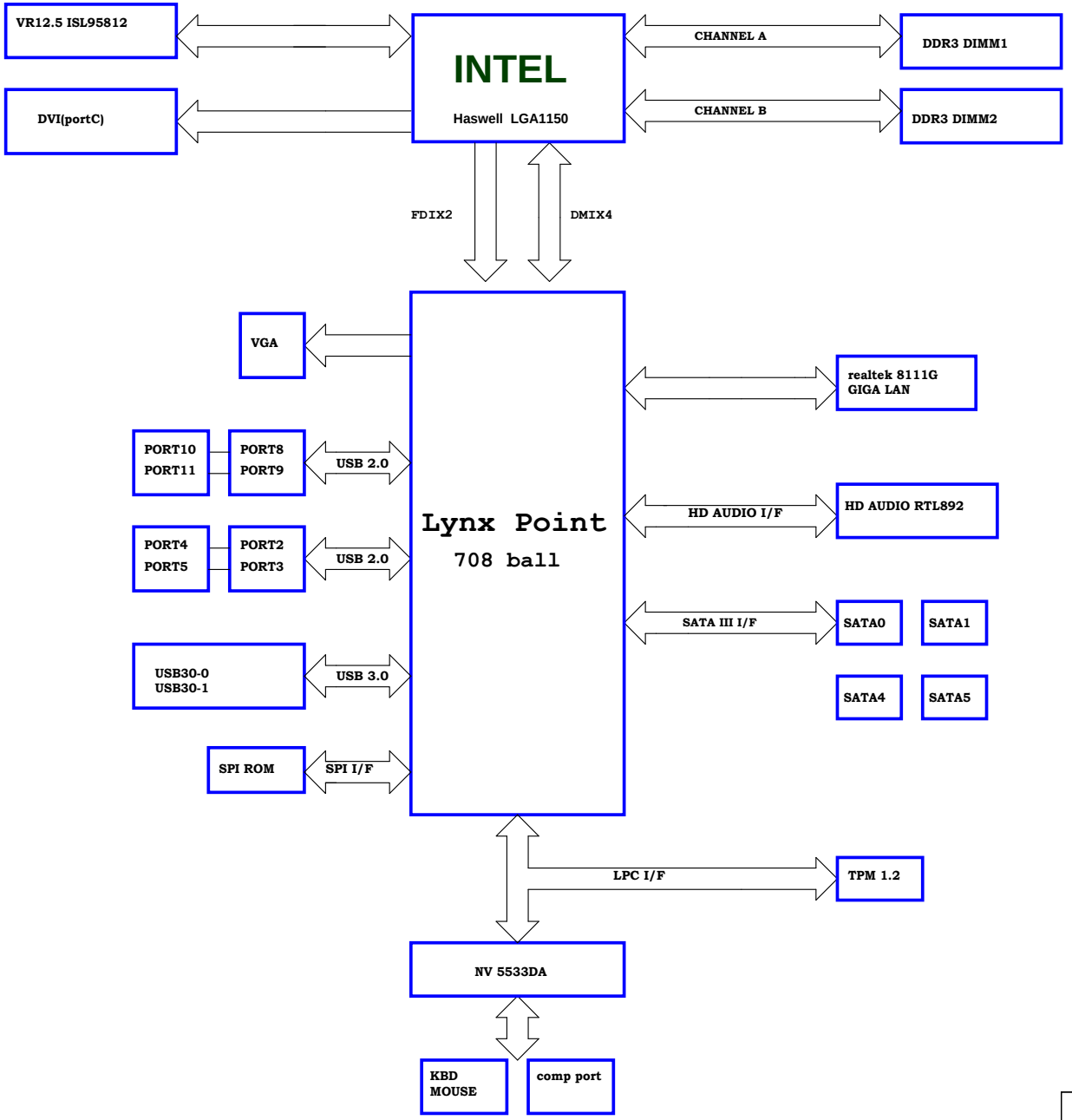
MS-7817

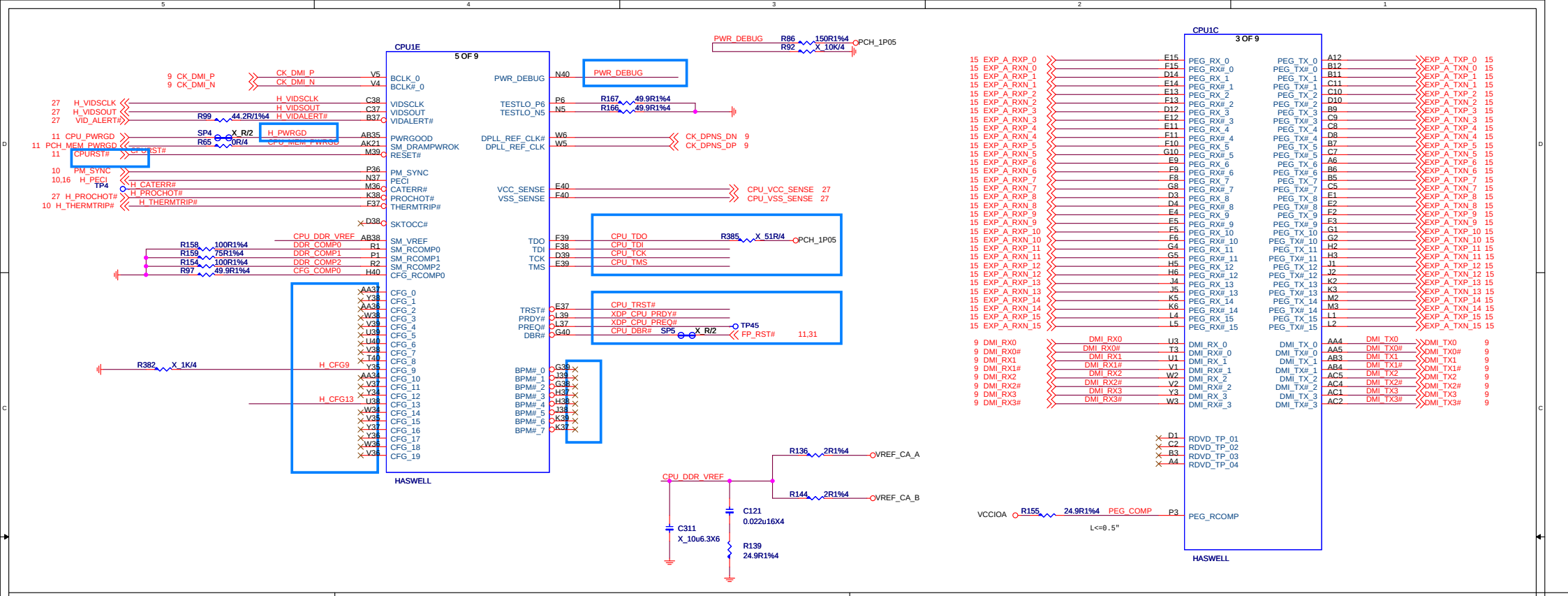
Size: Custom | Document Description: Cover Sheet | Rev: 30

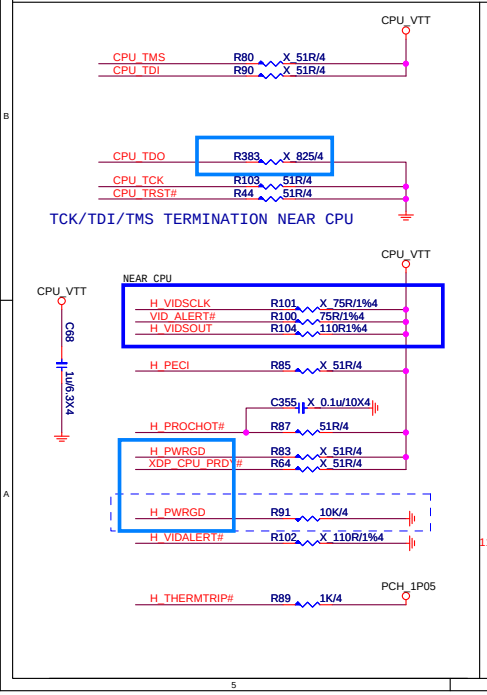
Date: Tuesday, September 17, 2013 | Sheet 1 of 36

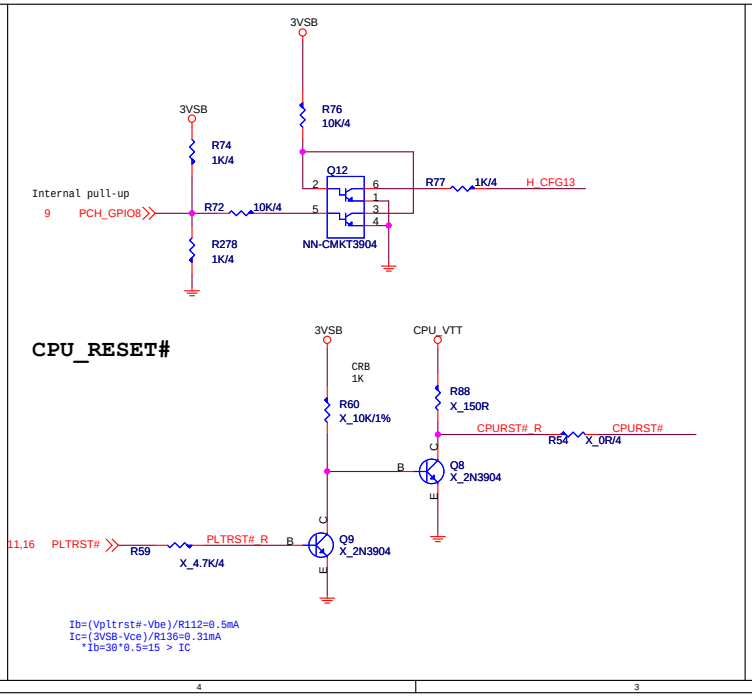
MS-7817 Block Diagram

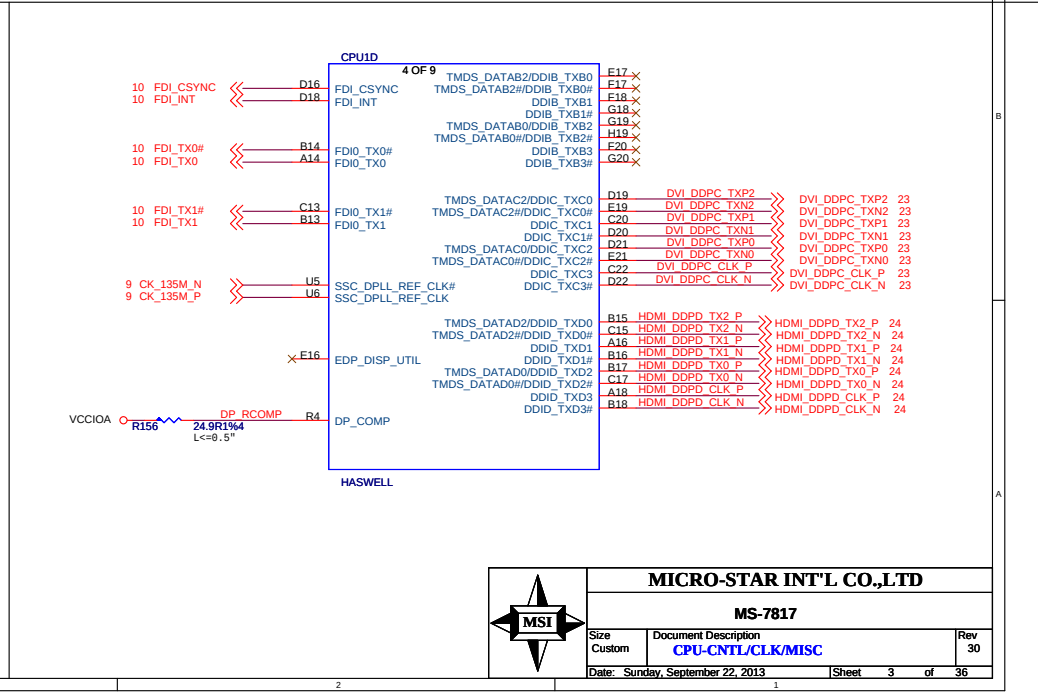


MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7817	
Size: Custom	Document Description: Block Diagram	Rev: 30
Date: Tuesday, September 17, 2013	Sheet 2 of 36	

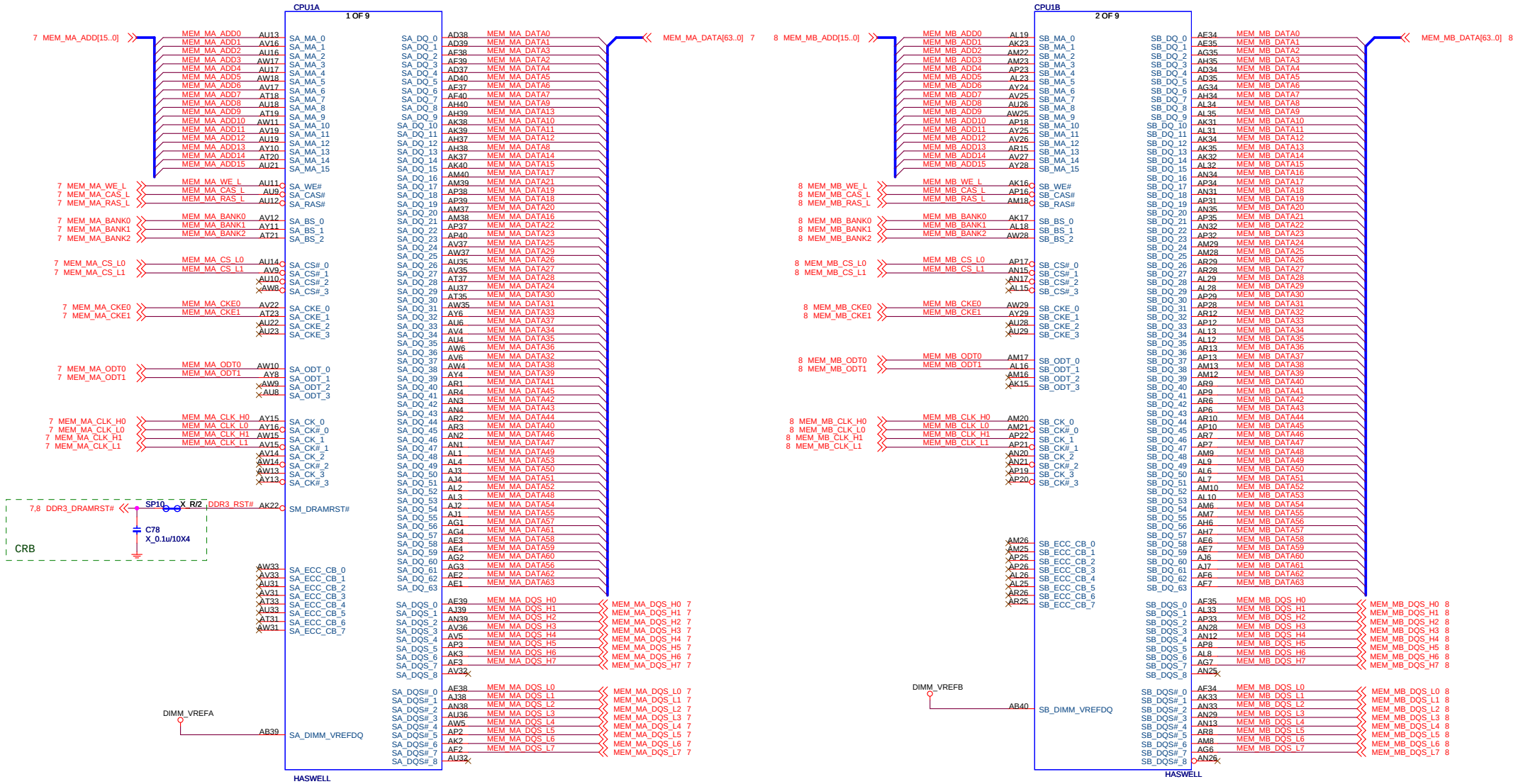




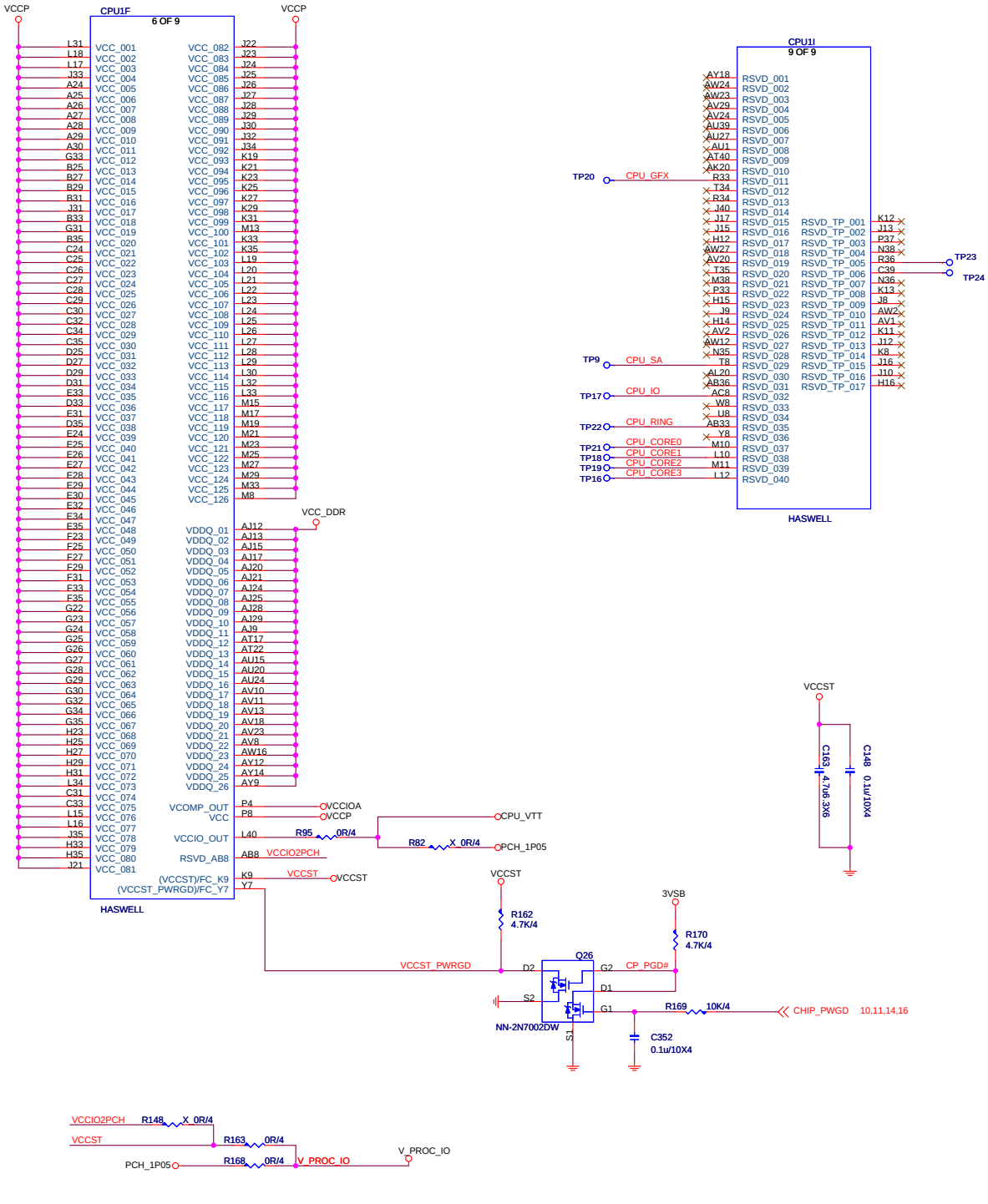




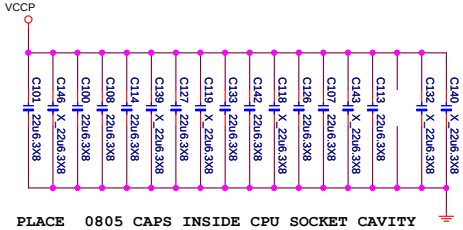
MICRO-STAR INT'L CO.,LTD	
MS-7817	
Size: Custom	Document Description: CPU-CNTL/CLK/MISC
Rev: 30	
Date: Sunday, September 22, 2013	Sheet 3 of 36



MICRO-STAR INT'L CO.,LTD		
MS-7817		
Size: Custom	Document Description: CPU-Memory	Rev: 30
Date: Wednesday, September 18, 2013	Sheet 4 of 36	

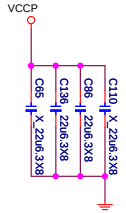


+CPU_VCCP-Decoupling

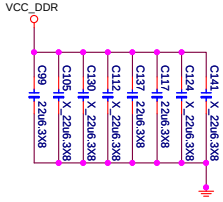


PLACE 0805 CAPS INSIDE CPU SOCKET CAVITY

PLACE 0805 CAPS Near CPU SOCKET edge

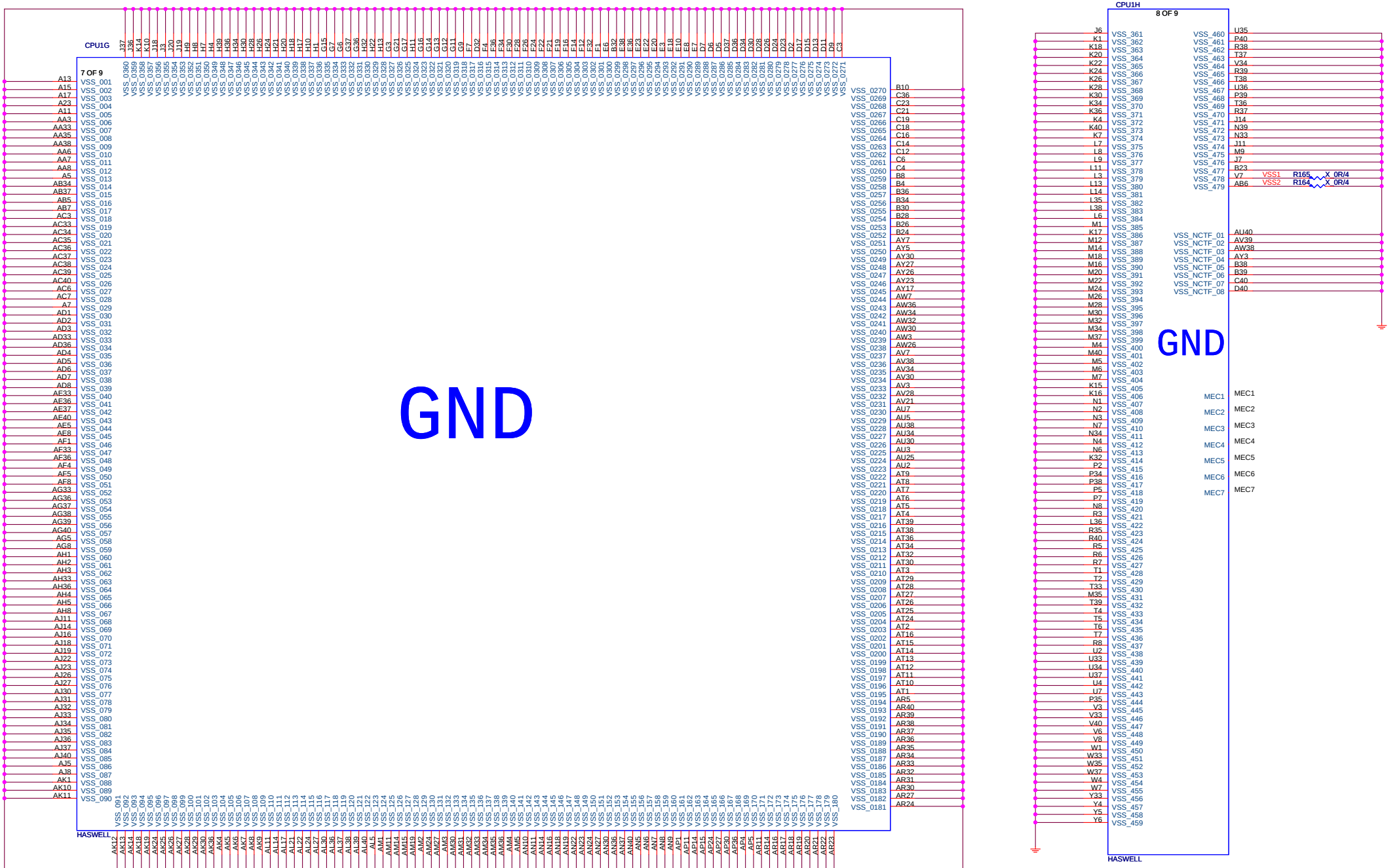


+1.5V_DDR3-Decoupling

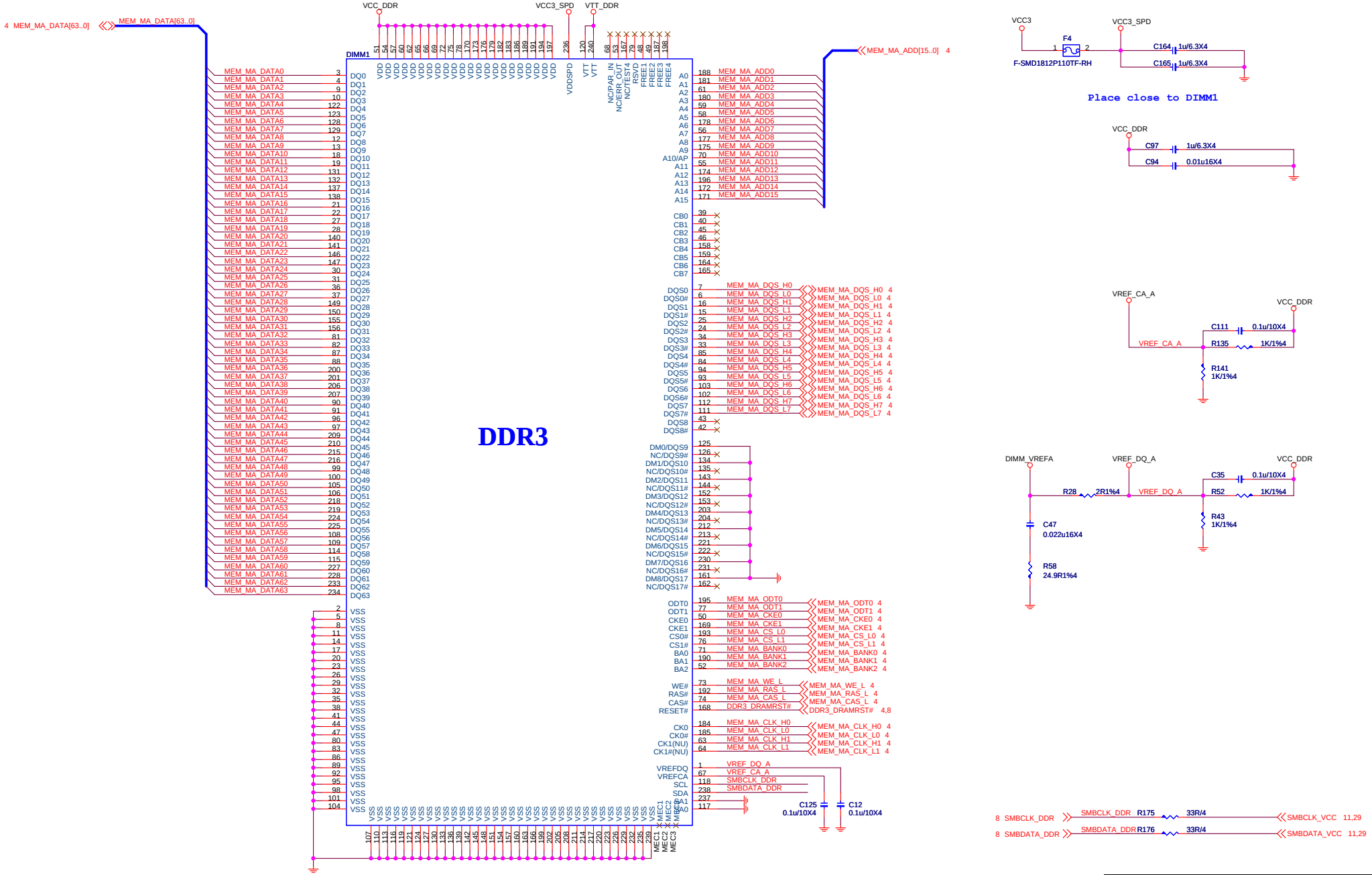


CPU SOCKET CAVITY CAPS

MICRO-STAR INT'L CO.,LTD		
MS-7817		
Size: Custom	Document Description: CPU-Power	Rev: 30
Date: Tuesday, September 17, 2013	Sheet 5 of 36	

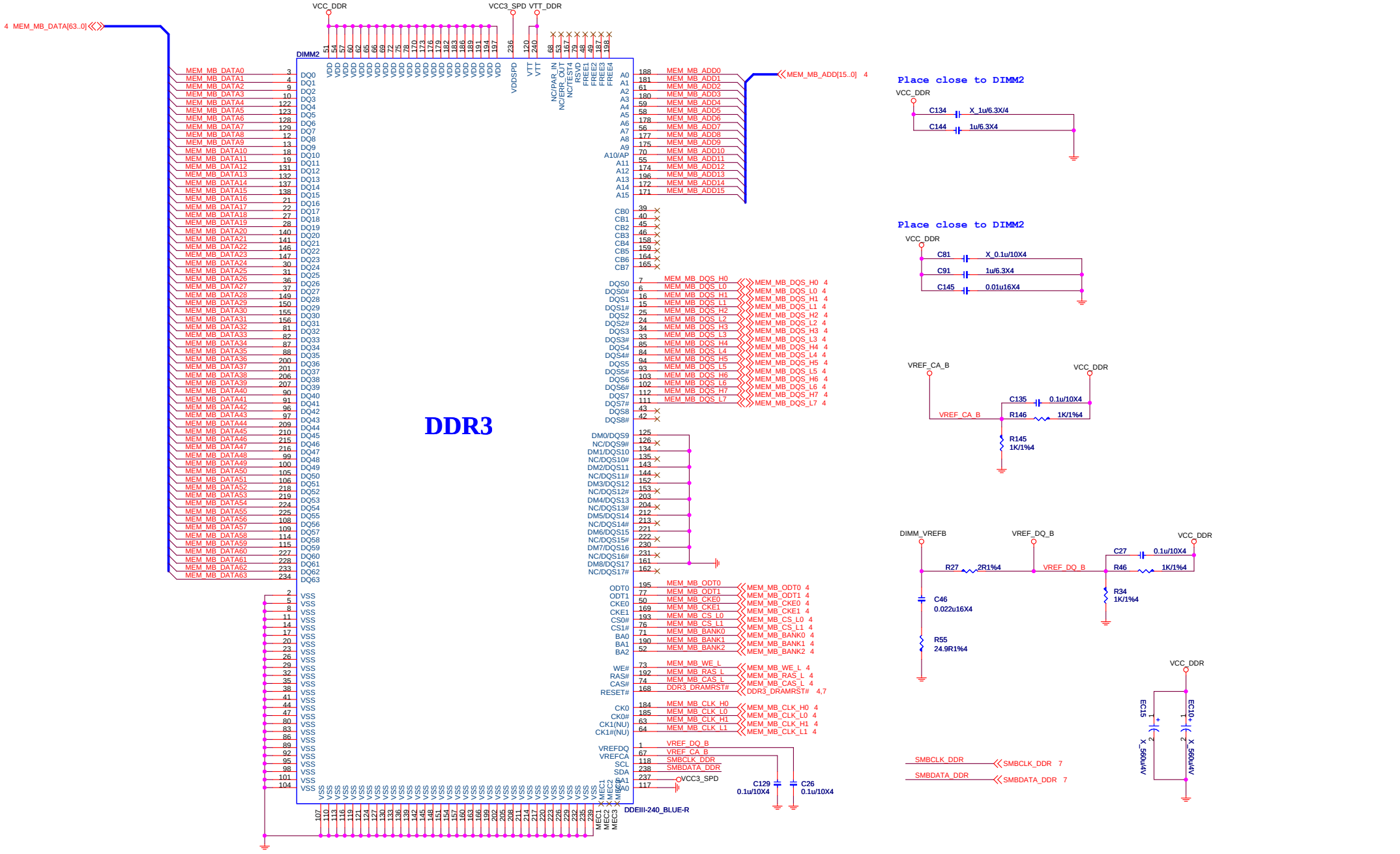


MICRO-STAR INT'L CO.,LTD			
MS-7817			
Size: Custom	Document Description: CPU-GND		Rev: 30
Date: Tuesday, September 17, 2013		Sheet 6 of 36	



MICRO-STAR INT'L CO.,LTD	
MS-7817	
Size: Custom	Document Description: DDR3 Chanel-A DIMM1/2
Rev: 30	
Date: Wednesday, September 18, 2013	Sheet 7 of 36

DDRIII DIMM_B0



MICRO-STAR INT'L CO.,LTD	
MS-7817	
Size: Custom	Document Description: DDR3 Chanel-B DIMM3/4
Rev: 30	
Date: Wednesday, September 18, 2013	Sheet 8 of 36

USB 2.0 ports 6,7,12 and 13 are disabled on 10 port SKUs.
Only USB 3.0 ports 1 and 2 are enabled.
pcie port7,8 NA

PCH1B

PCI-E

USB(2.0)

USB(3.0)

DMI

2 OF 8

LYNX

PCH1F

CLOCK

CLOCK_IN

6 OF 8

LYNX

Programmable output clock
to 33/48MHZ

EMC

PCH1A

PIRQ&GPIO

1 OF8

LYNX

OC 0-3 for usb 0-7
OC 7-4 for usb 8-13

default:OUTPUT

no clock gen pull down

OPT BOM:FOR BIOS USE

CRYSTAL:25MHZ

GPIO10	Sus	Native	Yes	No	No	Multiplexed with OC6#. When configured as GPIO, default direction is Input (GPI).

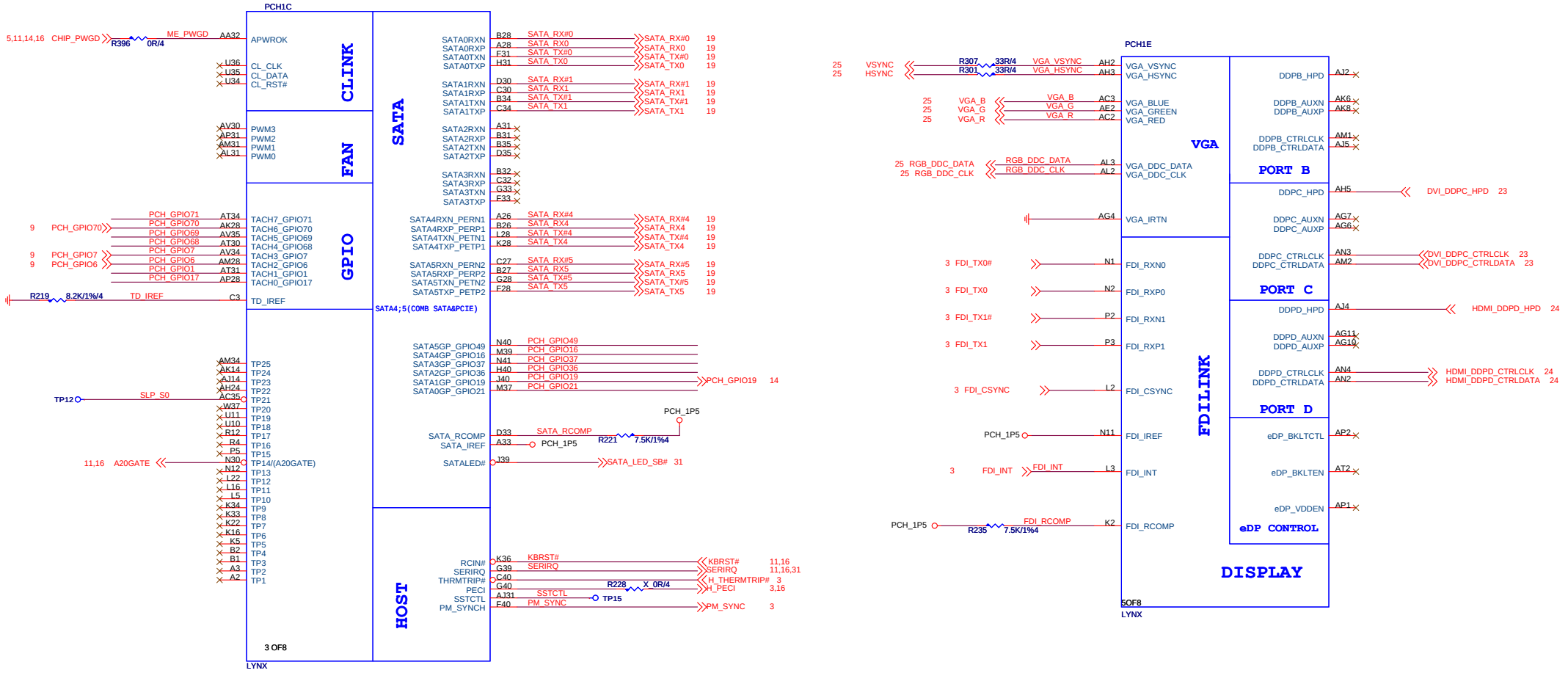
MICRO-STAR INT'L CO.,LTD

MS-7817

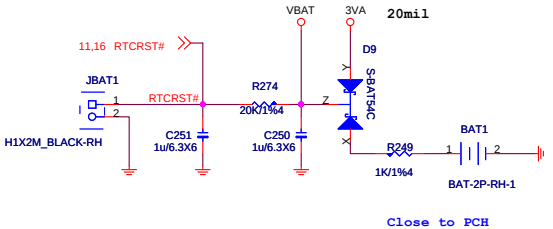
Size: Custom | Document Description: PPT PCIE/DMI/USB/CLK | Rev: 30

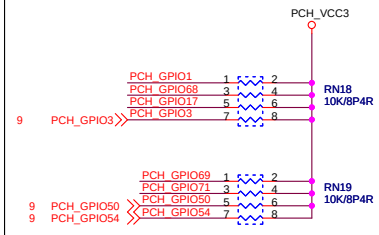
Date: Wednesday, October 09, 2013 | Sheet 9 of 36

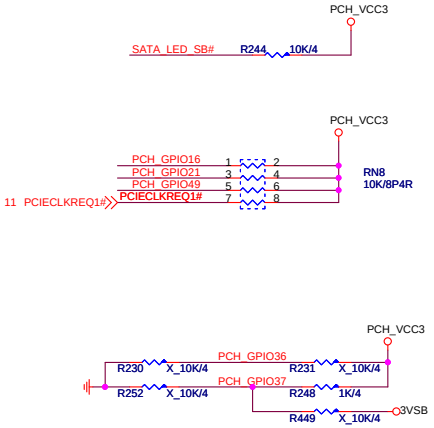
SATA ports 2 and 3 are disabled on 4 port SKUs.
SATA 6 Gb/s support on ports 0 and 1 only.



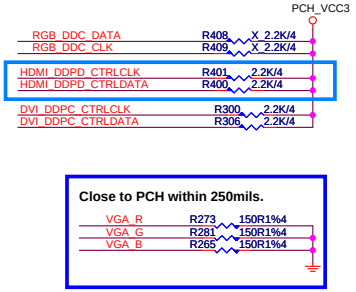
RTC and CLR_CMOS







Enable VGA(CTRLCLK/DATA Pull High)

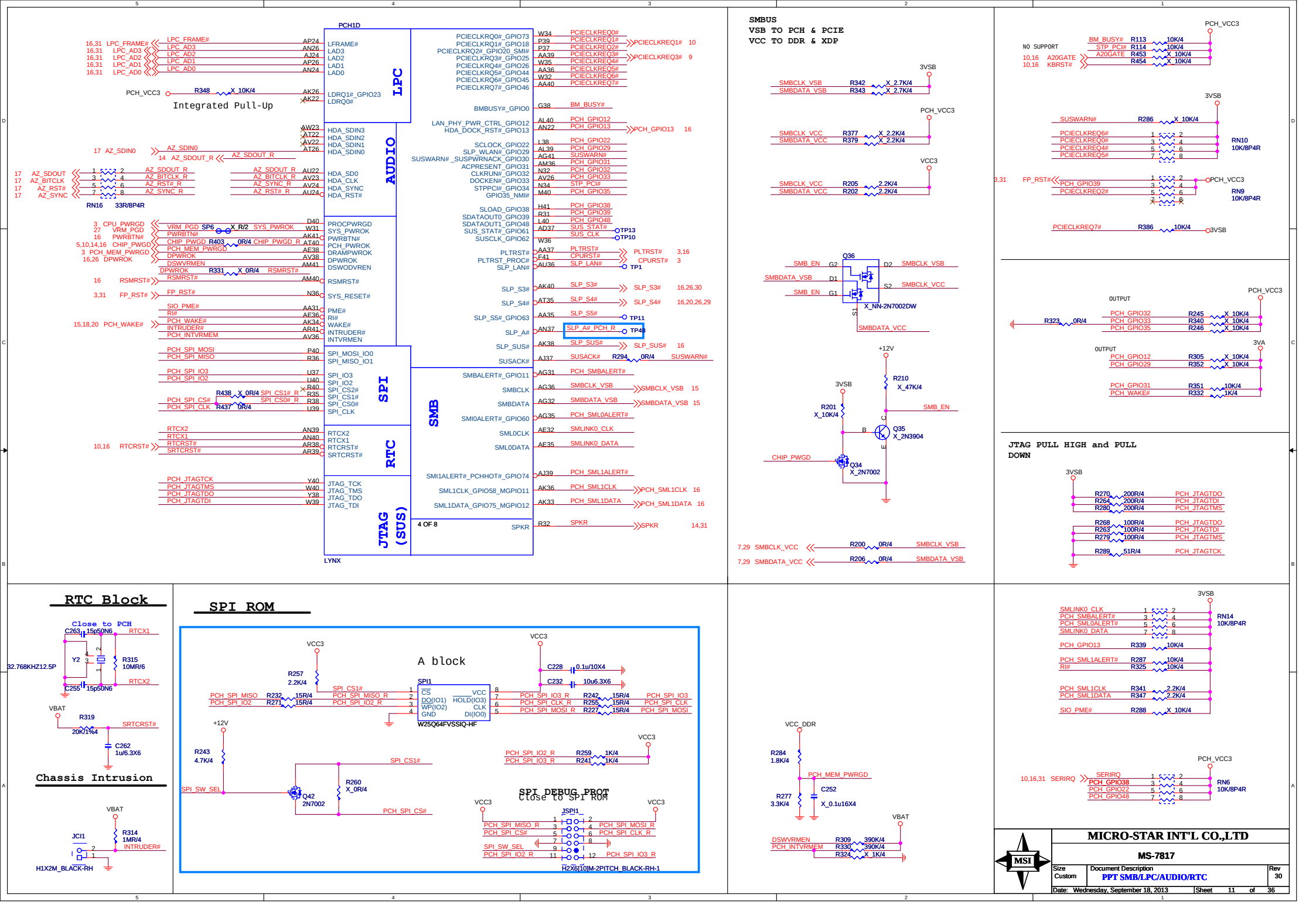


MICRO-STAR INT'L CO.,LTD

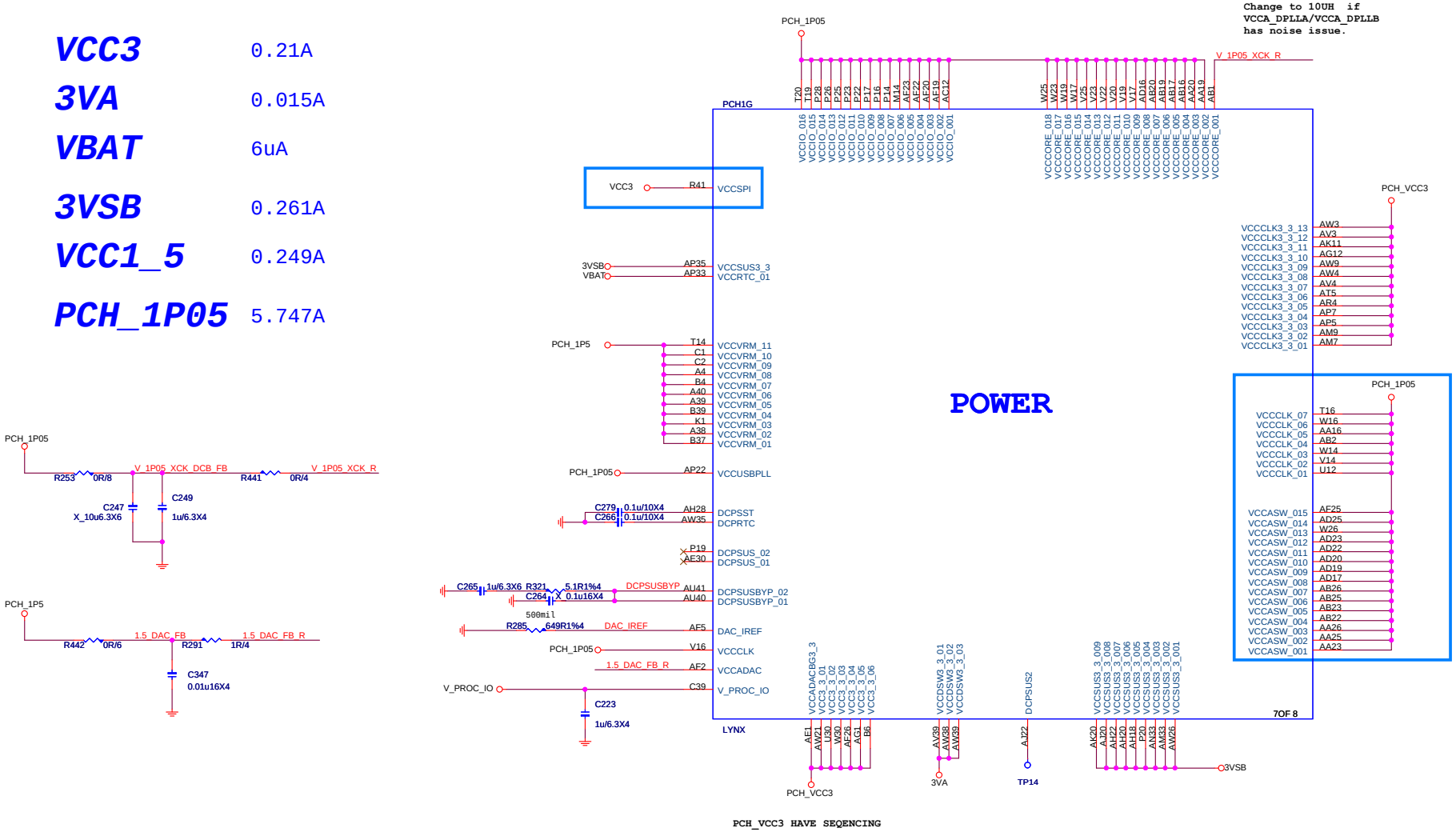
MS-7817

Size	Document Description	Rev
Custom	PPT SATA/HOST/FAN/GPIO/VGA	30

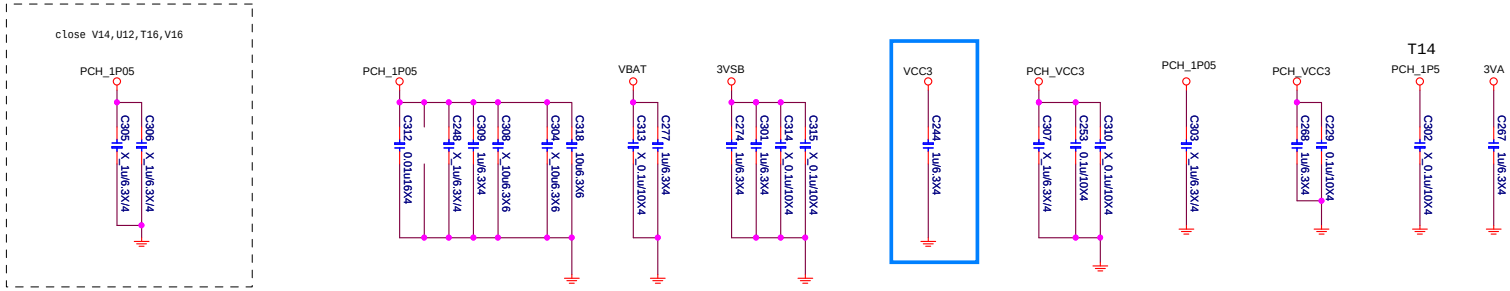
Date: Thursday, October 10, 2013 Sheet 10 of 36


PCH1D
LPC
AUDIO
SPI
RTC
JTAG (SUS)
SMB
LYNX
4 OF 8
Integrated Pull-Up
SMBUS
VSB TO PCH & PCIE
VCC TO DDR & XDP
JTAG PULL HIGH and PULL DOWN
RTC Block
Close to PCH
Chassis Intrusion
SPI ROM
A block
SPI DEBUG PROT
Close to SPI ROM
MICRO-STAR INT'L CO.,LTD
MS-7817
PPT SMB/LPC/AUDIO/RTC
Size Custom
Rev 30
Date: Wednesday, September 18, 2013
Sheet 11 of 36

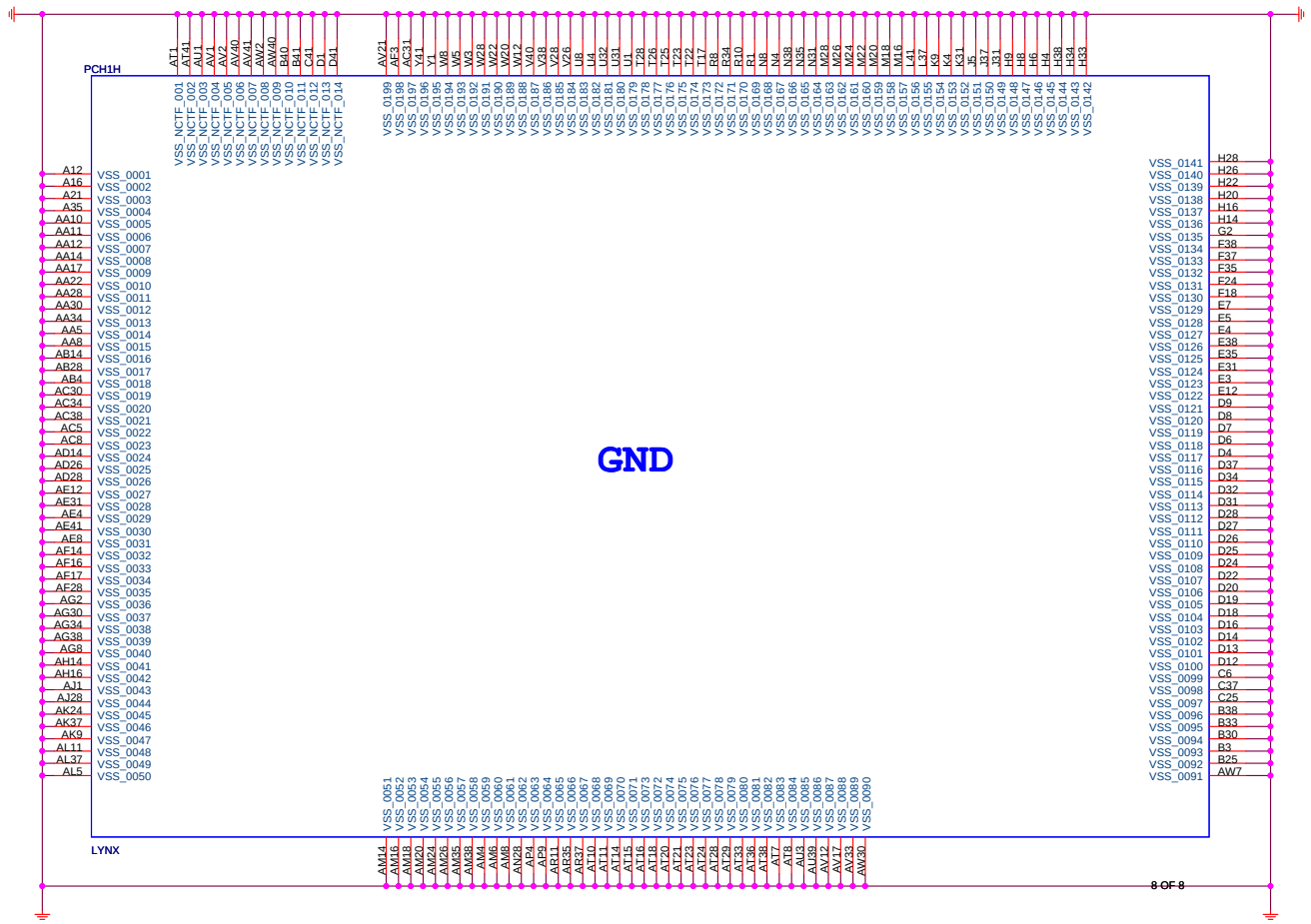
VCC3	0.21A
3VA	0.015A
VBAT	6uA
3VSB	0.261A
VCC1_5	0.249A
PCH_1P05	5.747A



PCH decoupling cap

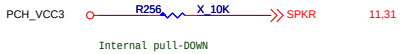


MICRO-STAR INT'L CO.,LTD		
MS-7817		
Size: Custom	Document Description: LYNX -POWER PIN	Rev: 30
Date: Tuesday, September 17, 2013	Sheet 12 of 36	



MICRO-STAR INT'L CO.,LTD		
MS-7817		
Size: Custom	Document Description: PPT GND/NVRAM	Rev: 30
Date: Tuesday, September 17, 2013	Sheet 13 of 36	

PCH Straps



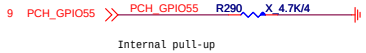
SPKR

Default Mode:

Internal weak Pull-down.

No Reboot Mode with TCO Disabled:

Connect to Vcc3_3 with 8.2k-10k Ohm weak pullup resistor.



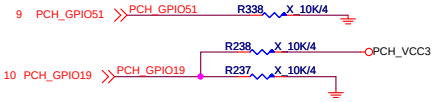
GPIO55

Default Mode:

Internal pull-up.

Top Block Swap Mode:

Connect to ground with 4.7k Ohm weak pulldown resistor.



SATA1GP/GPIO19, GPIO51

Default (SPI):

Left both SATA1GP/GPIO19 and GPIO51 floating.
No pull up required.

Boot from PCI:

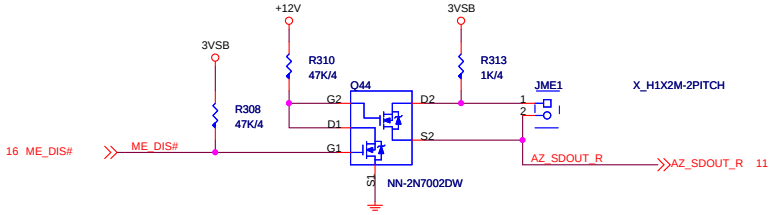
Connect SATA1GP/GPIO19 to ground with 1k Ohm pull-down resistor.
Leave GPIO51 Floating.

Boot from LPC:

Connect both SATA1GP/GPIO19 and GPIO51 to ground with 1k Ohm pull-down resistor.

GPIO53

Do not pull low.
Connect to ground with 1k Ohm pull-down resistor.



HDA_SDO

Default:

Do not pull high.

Disable ME in Manufacturing Mode:

Connect to VccSusHDA with 1k Ohm pull-up resistor through a jumper.

GPIO37

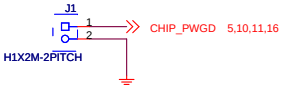
Enable TLS:

Pull up with 1k Ohm to VccSus3.3.

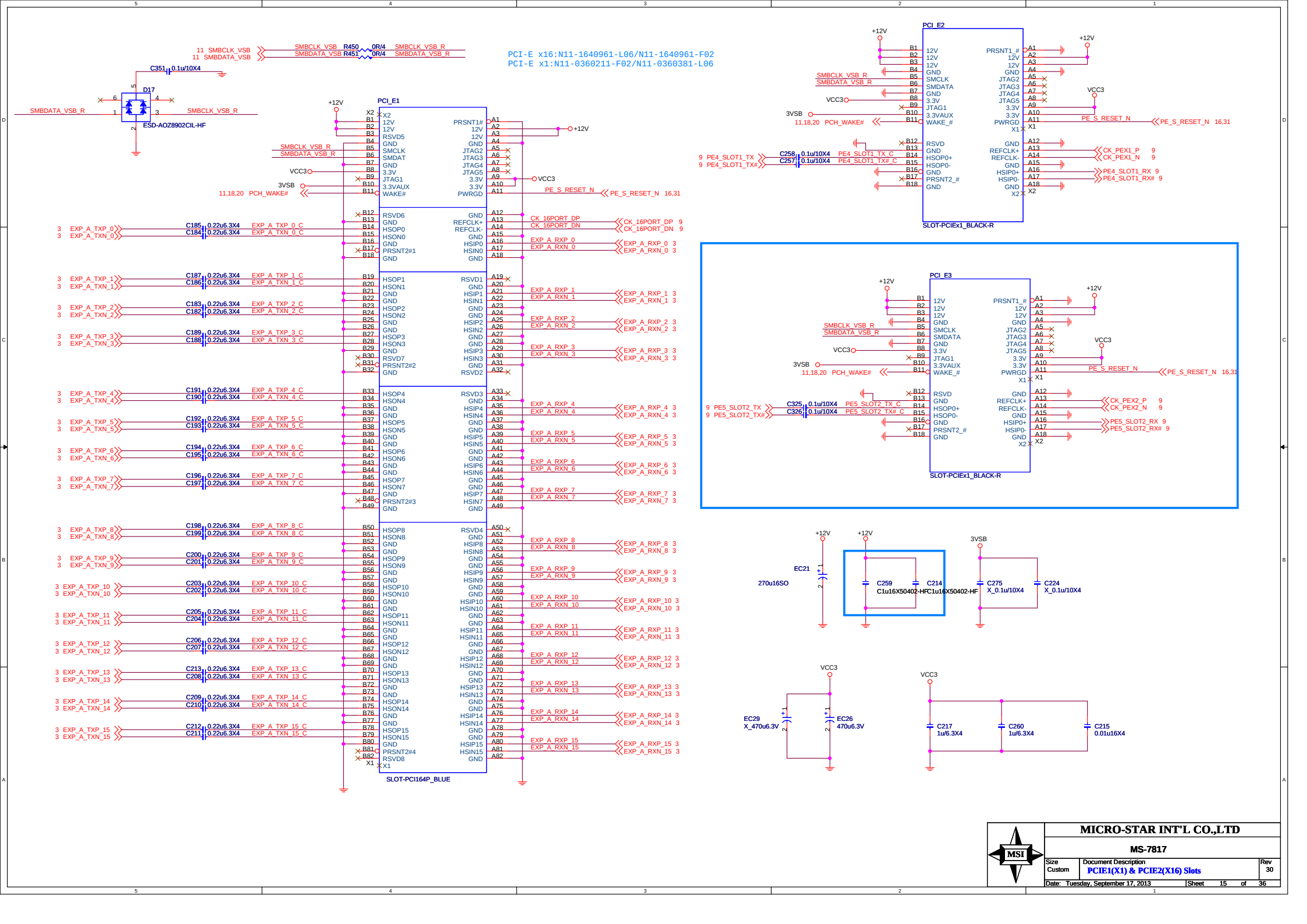
Default (Disable TLS):

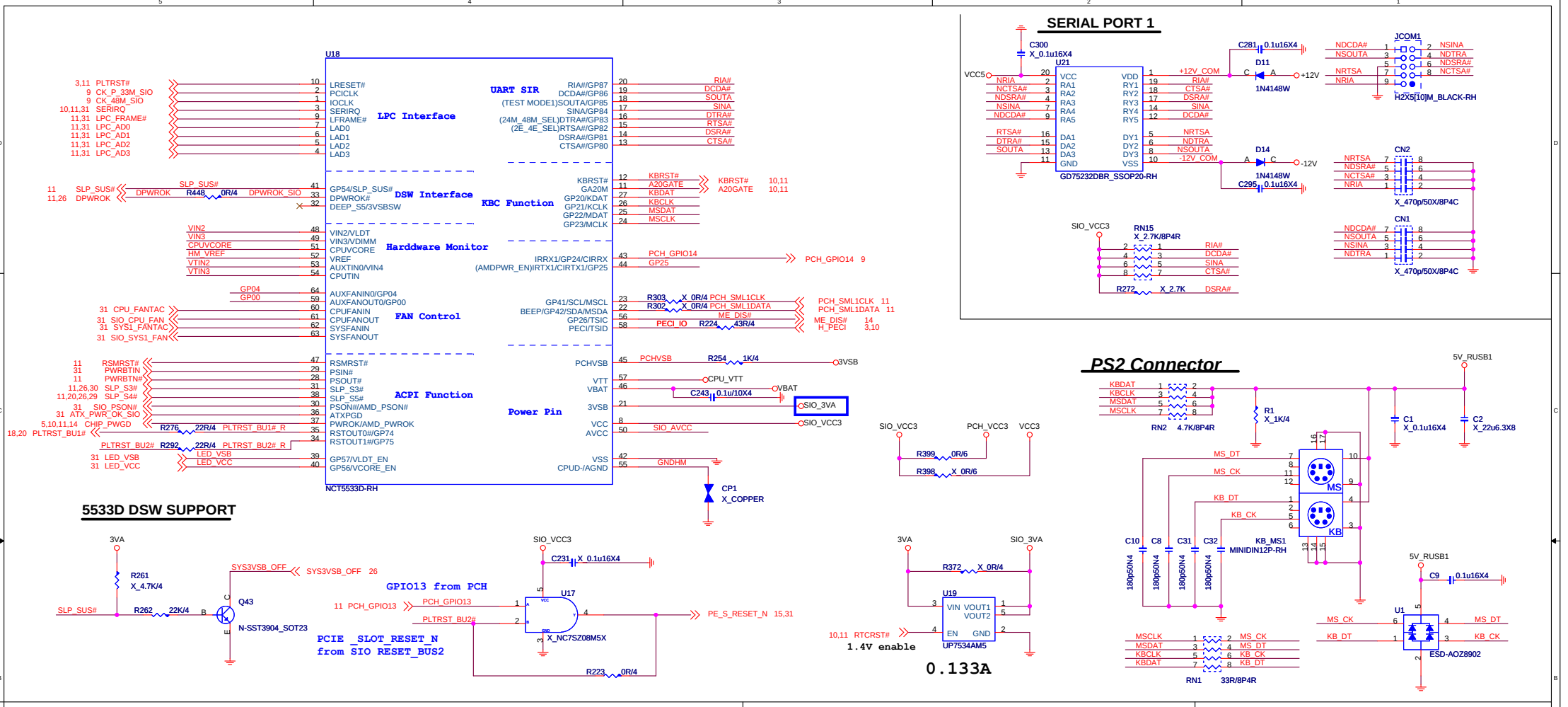
Leave NC. Internal pull down.

For test cpu voltage



MICRO-STAR INT'L CO.,LTD		
MS-7817		
Size: Custom	Document Description: PPT STRAPS	Rev: 30
Date: Tuesday, September 17, 2013	Sheet 14 of 36	


PCI-E x16:N11-1640961-L06/N11-1640961-F02
PCI-E x1:N11-0360211-F02/N11-0360381-L06
PCI_E1
SLOT-PCI164P_BLUE
PCI_E2
SLOT-PCIEx1_BLACK-R
PCI_E3
SLOT-PCIEx1_BLACK-R
ESD-AOZ8902CIL-HF
MICRO-STAR INT'L CO.,LTD
MS-7817
PCIE1(X1) & PCIE2(X16) Slots
Size Custom
Rev 30
Date: Tuesday, September 17, 2013
Sheet 15 of 36



PIN	Function	NET Name	HI	LO
44	AMDPWR_EN		ENABLE AMD PWR SEQ	DISABLE AMD PWR SEQ
18	TEST_MODE1	SOUTA	TEST MODE 1 ENABLE	TEST MODE 1 DISABLE
16	24M_48M_SEL	DTRA#	48MHz	24MHz
15	2E_4E_SEL	RTSA#	4E	2E

MICRO-STAR INT'L CO.,LTD

MS-7817

Size: Custom | Document Description: SIO-NUVOTON NCT5533D | Rev: 30

Date: Sunday, September 29, 2013 | Sheet 16 of 36

Type C:
ALC887-VD
VT1708S CE

11mA
Closed Codec

CA4 closed PIN25
CA3 closed PIN38

SMD CAP: Fail to test THD+N
EL/SOLID cap: Test THD+N will Pass

45.8mA

100pF Cap can change to TVS by PM request.

Close to Front panel
For HDA/AC97 front cable.

Closed Codec

CA17 Reserve for 1708

887: Remove
1708:Stuff

EMI

0R for cost down

CA33,CA34 close to LA1

Rear Line OUT De-POP circuit

(reserve de-pop circuit for Rear Line out & Front Headphone out)

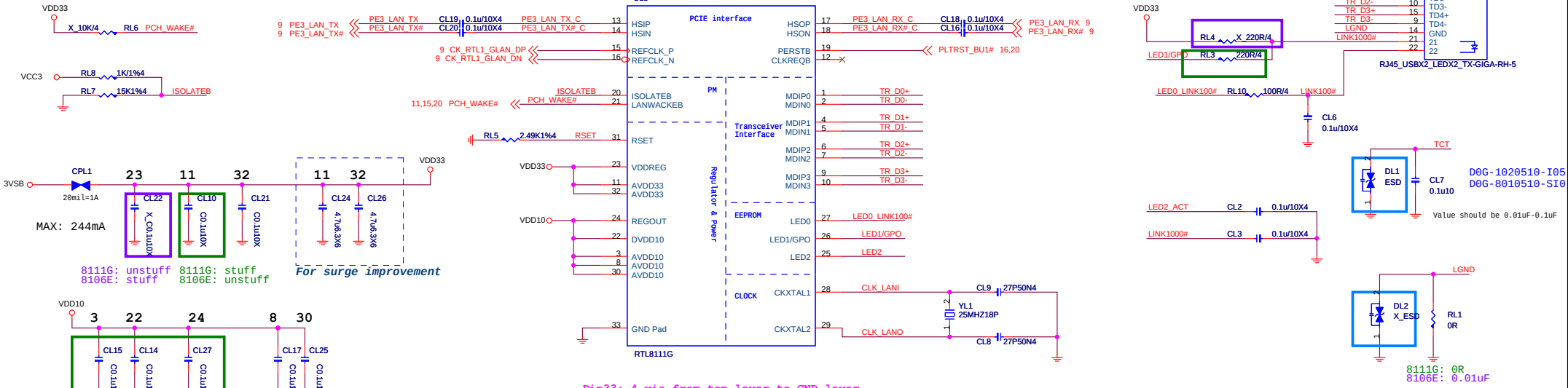
Digital

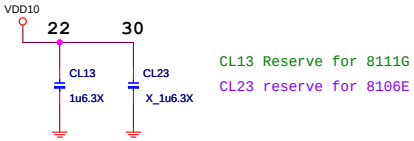
Analog

MICRO-STAR INT'L CO.,LTD			
MS-7817			
Size: Custom	Document Description: Audio Codec ALC892/887		Rev: 30
Date: Tuesday, September 17, 2013	Sheet 17 of 36		

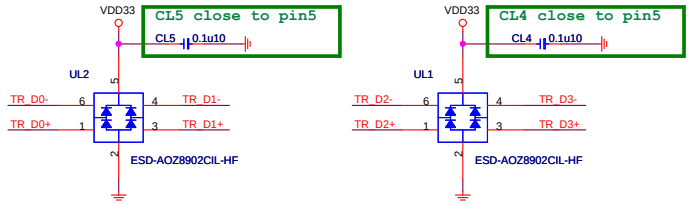
RTL8111G Giga LAN

RTL8106E 10/100M LAN





Reserve ESD Protect



MSI P/N : D0G-0200529-A68 Vender P/N : AOZ8902CI
MSI P/N : D0G-0100619-I05 Vender P/N : TVLST2304AD0

8106E POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	15/94	49.5/310.2
100 M Idle/TxRx	52/105	171.6/346.5
S0 ALDPS	4	13.2

8111G POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

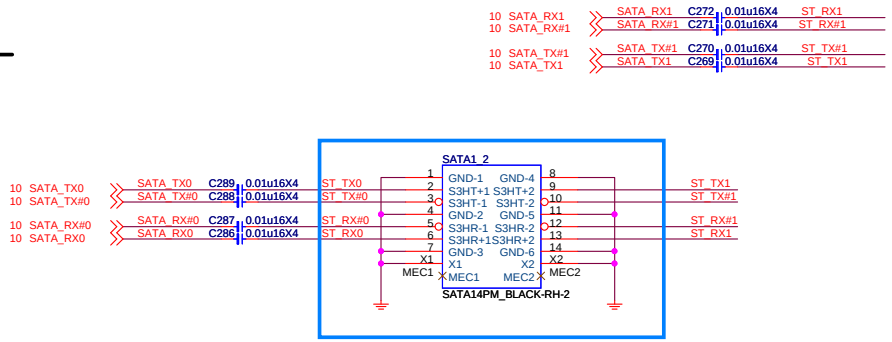
MICRO-STAR INT'L CO.,LTD

MS-7817

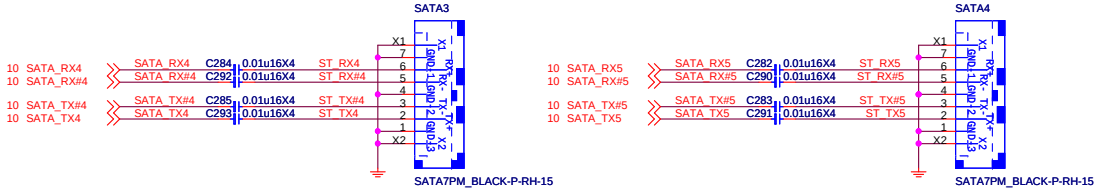
Size	Document Description	Rev
Custom	LAN RTL8111G/8106E	30

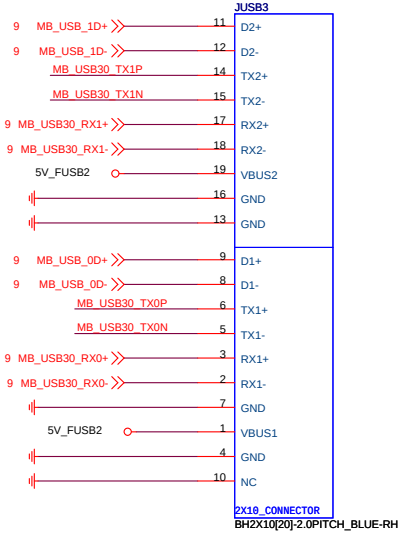
Date: Sunday, September 22, 2013 Sheet 18 of 36

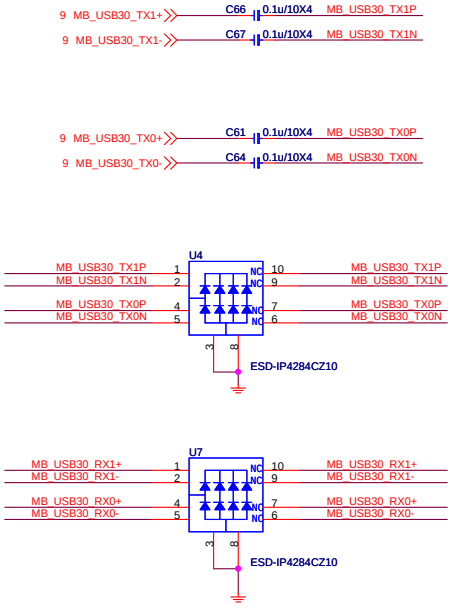
SATA 6G PORT 0,1

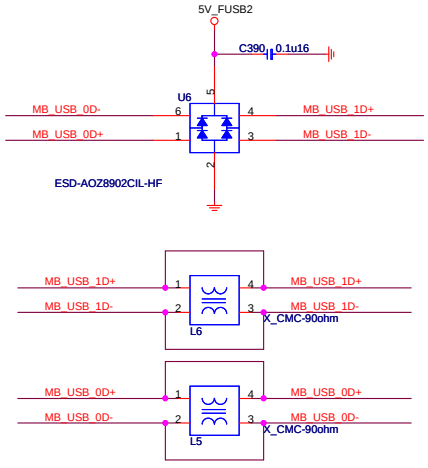


SATA 3G PORT 4,5

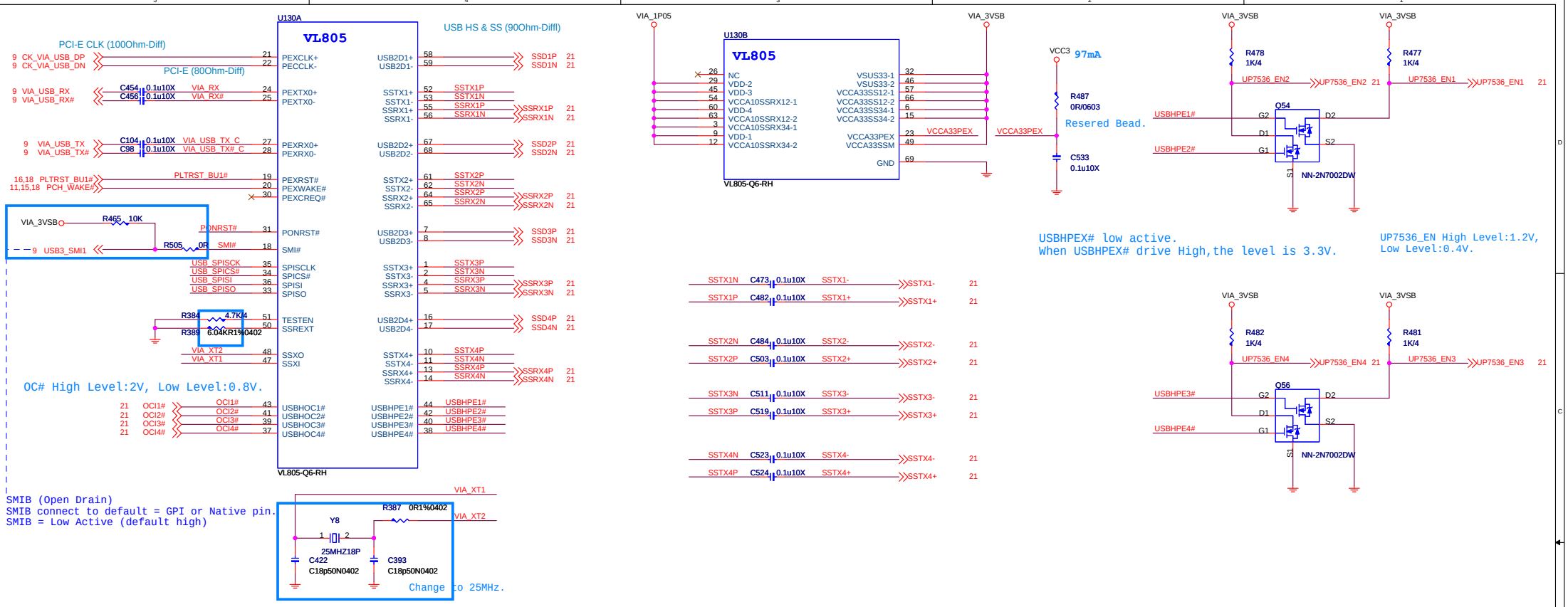


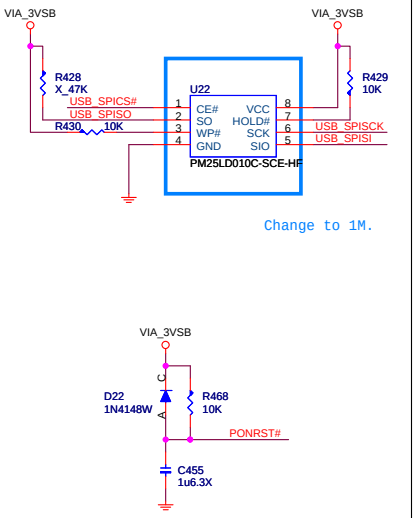


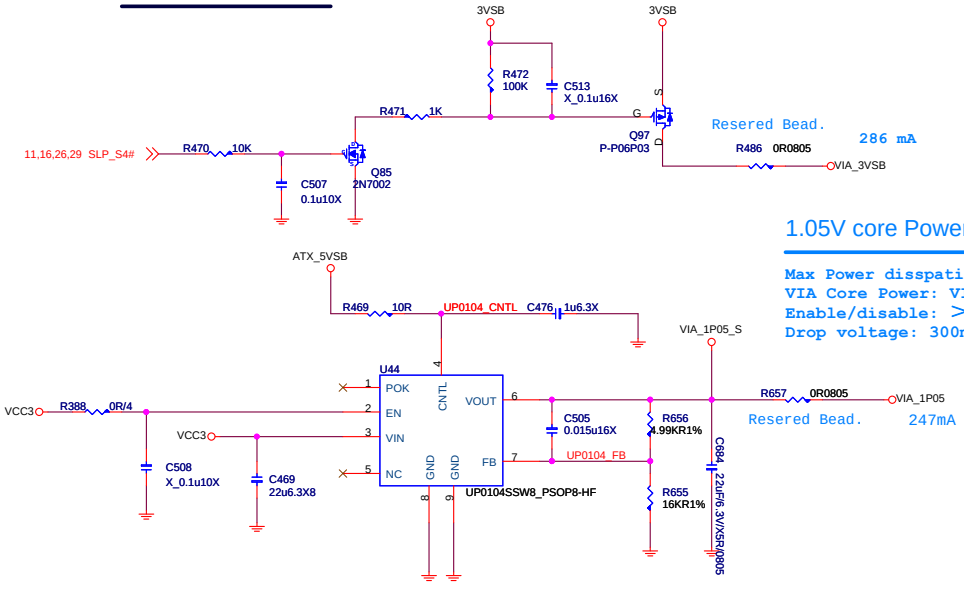




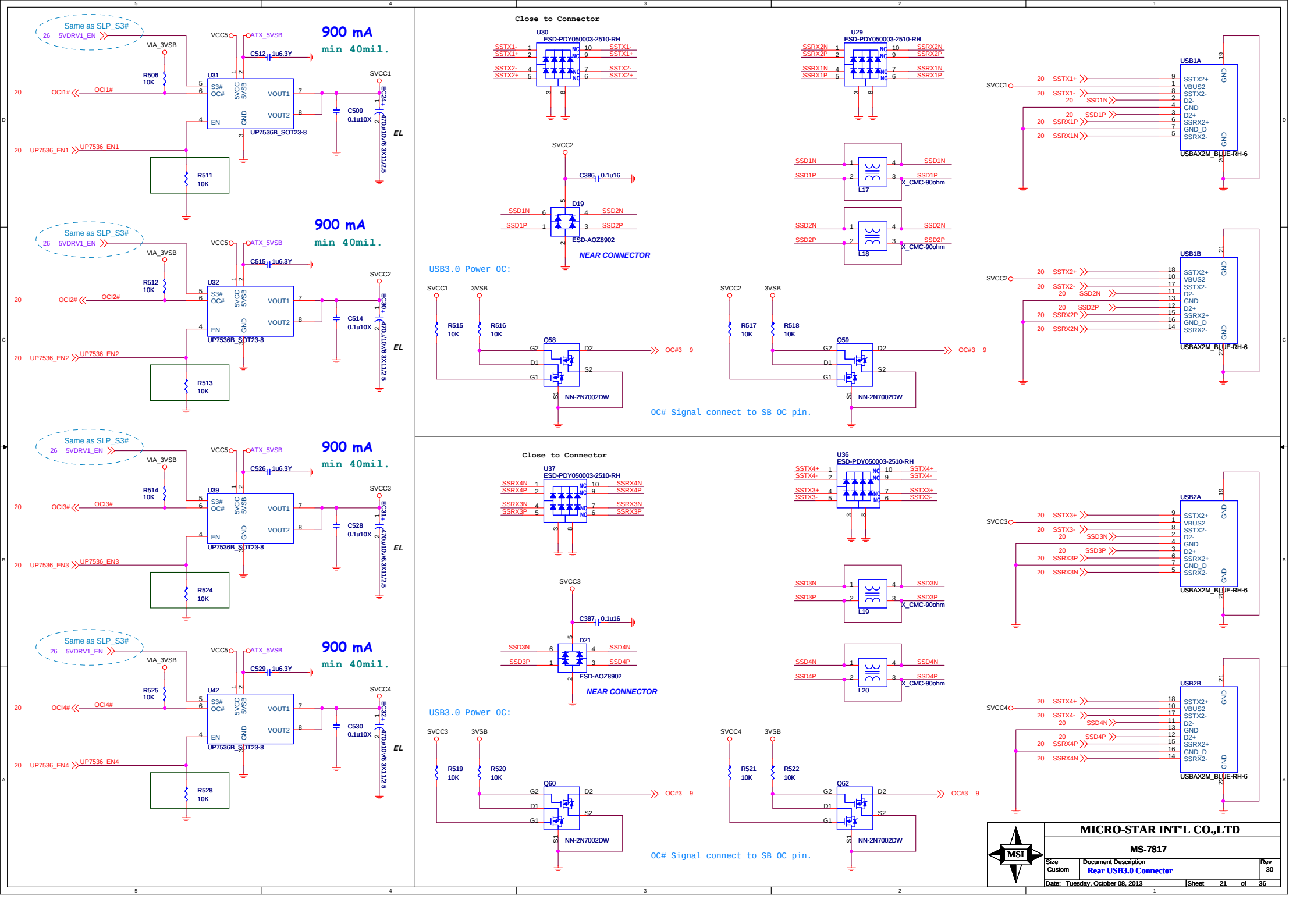
MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7817	
Size: Custom	Document Description: SATA Connector	Rev: 30
Date: Monday, October 07, 2013	Sheet 19 of 36	







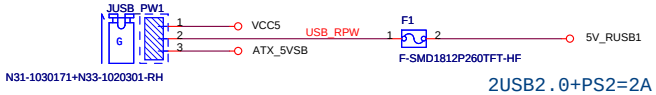
MICRO-STAR INT'L CO.,LTD	
MS-7817	
Size: Custom	Document Description: VL805-USB 3.0 Host
Rev: 30	
Date: Wednesday, October 09, 2013	Sheet 20 of 36


Same as SLP_S3#
26 5VDRV1_EN
VIA_3VSB
VCC5
ATX_5VSB
900 mA
min 40mil.
R506 10K
U31
S3#
OC#
5VCC
5VSB
VOUT1
VOUT2
GND
EN
UP7536B_SOT23-8
C512 1u6.3Y
SVCC1
EC24+
470u/10v/6.3X11/2.5
C509 0.1u10X
EL
20 OCI1# OCI1#
20 UP7536_EN1 UP7536_EN1
R511 10K
Same as SLP_S3#
26 5VDRV1_EN
VIA_3VSB
VCC5
ATX_5VSB
900 mA
min 40mil.
R512 10K
U32
UP7536B_SOT23-8
C515 1u6.3Y
SVCC2
EC30+
470u/10v/6.3X11/2.5
C514 0.1u10X
EL
20 OCI2# OCI2#
20 UP7536_EN2 UP7536_EN2
R513 10K
Same as SLP_S3#
26 5VDRV1_EN
VIA_3VSB
VCC5
ATX_5VSB
900 mA
min 40mil.
R514 10K
U39
UP7536B_SOT23-8
C526 1u6.3Y
SVCC3
EC31+
470u/10v/6.3X11/2.5
C528 0.1u10X
EL
20 OCI3# OCI3#
20 UP7536_EN3 UP7536_EN3
R524 10K
Same as SLP_S3#
26 5VDRV1_EN
VIA_3VSB
VCC5
ATX_5VSB
900 mA
min 40mil.
R525 10K
U42
UP7536B_SOT23-8
C529 1u6.3Y
SVCC4
EC32+
470u/10v/6.3X11/2.5
C530 0.1u10X
EL
20 OCI4# OCI4#
20 UP7536_EN4 UP7536_EN4
R528 10K
Close to Connector
U30
ESD-PDY050003-2510-RH
SSTX1-
SSTX1+
SSTX2-
SSTX2+
SVCC2
C386 0.1u16
D19
SSD1N
SSD1P
SSD2N
SSD2P
ESD-AOZ8902
NEAR CONNECTOR
USB3.0 Power OC:
SVCC1
3VSB
R515 10K
R516 10K
Q58
G2
D1
G1
D2
S2
S1
NN-2N7002DW
OC#3 9
U29
ESD-PDY050003-2510-RH
SSRX2N
SSRX2P
SSRX1N
SSRX1P
L17
L18
X_CMC-90ohm
USB1A
USB1B
USBAX2M_BLUE-RH-6
SSTX1+
SSTX1-
SSD1N
SSD1P
SSRX1P
SSRX1N
SSTX2+
SSTX2-
SSD2N
SSD2P
SSRX2P
SSRX2N
SVCC2
R517 10K
R518 10K
Q59
OC# Signal connect to SB OC pin.
Close to Connector
U37
ESD-PDY050003-2510-RH
SSRX4N
SSRX4P
SSRX3N
SSRX3P
SVCC3
C387 0.1u16
D21
SSD3N
SSD3P
SSD4N
SSD4P
ESD-AOZ8902
NEAR CONNECTOR
USB3.0 Power OC:
SVCC3
3VSB
R519 10K
R520 10K
Q60
OC#3 9
U36
ESD-PDY050003-2510-RH
SSTX4+
SSTX4-
SSTX3+
SSTX3-
L19
L20
X_CMC-90ohm
USB2A
USB2B
USBAX2M_BLUE-RH-6
SSTX3+
SSTX3-
SSD3N
SSD3P
SSRX3P
SSRX3N
SSTX4+
SSTX4-
SSD4N
SSD4P
SSRX4P
SSRX4N
SVCC4
R521 10K
R522 10K
Q62
OC# Signal connect to SB OC pin.
MICRO-STAR INT'L CO.,LTD
MS-7817
Size
Custom
Document Description
Rear USB3.0 Connector
Rev
30
Date: Tuesday, October 08, 2013
Sheet 21 of 36

Type C: jumper +Fuse

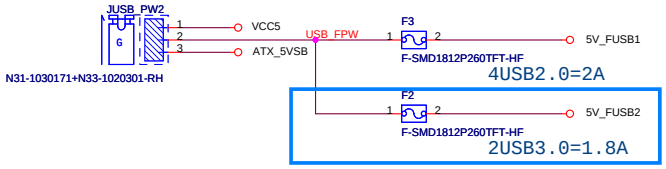
PCH/FCH side: OC# pull high to +3VSB

Near Rear ==>



2USB2.0+PS2=2A

Near Front ==>

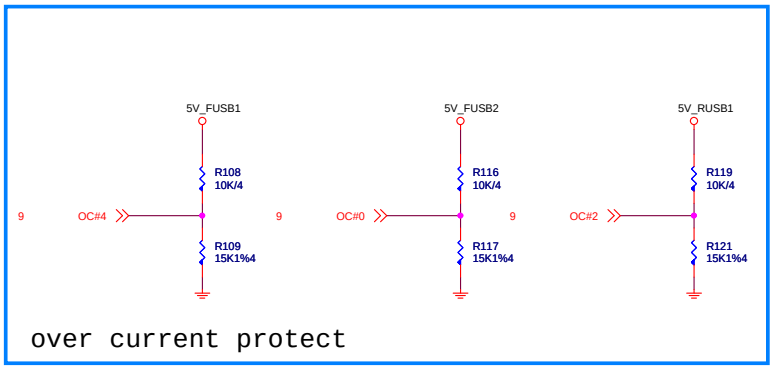


4USB2.0=2A

2USB3.0=1.8A

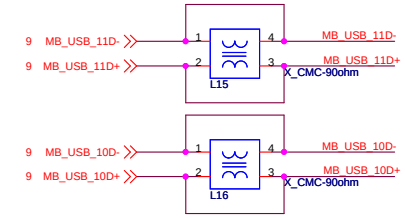
Default VCC5 (PIN1-2)

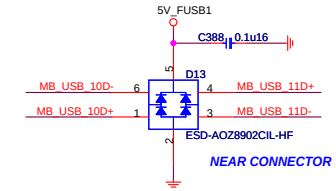
JUSB_PW	BIOS Menu	Wake up support
1-2	EUP Enable	Not support
	EUP Disable	
2-3	EUP Enable	Not support
	EUP Disable	support



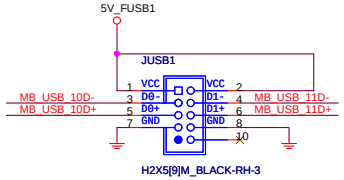
D08-2000300-P16 (Itrip=3.5A; 0.003ohm) support 6 USB ports (3A)
D08-0300700-P16 (Itrip=2.6A; 0.015ohm) support 4 USB ports (2A)
D08-0100110-P16 (Itrip=1.1A; 0.04ohm) support 2 usb 2.0 ports (1A)

FRONT USB PORT 8,9

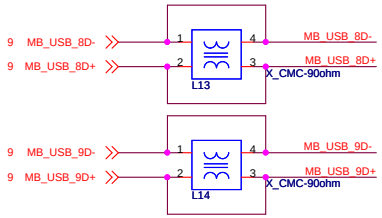


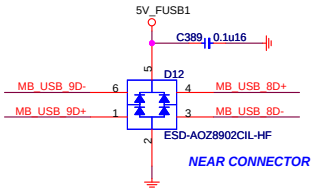


NEAR CONNECTOR



FRONT USB PORT 10.11





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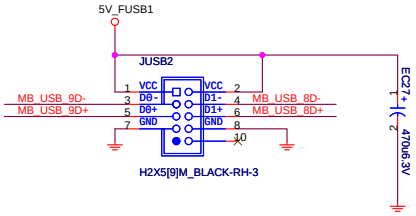
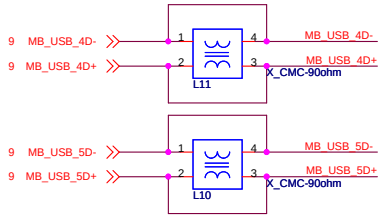
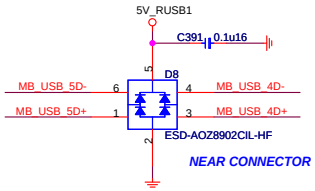
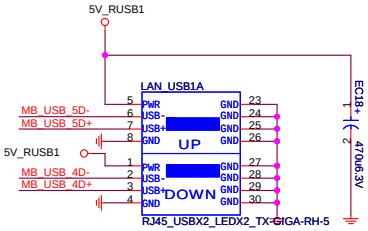


FRONT USB PORT 4.5





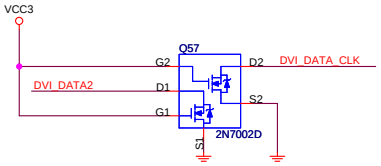
NEAR CONNECTOR

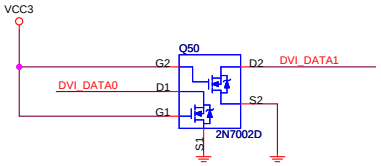


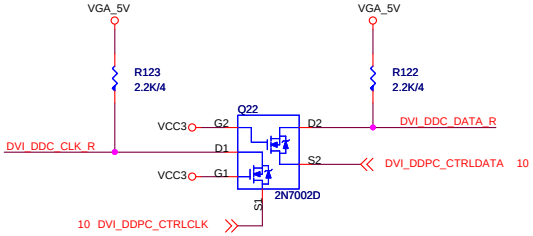
MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7817	
Size: Custom	Document Description: Rear I/O & USB2.0 Connector	Rev: 30
Date: Wednesday, October 09, 2013	Sheet 22 of 36	

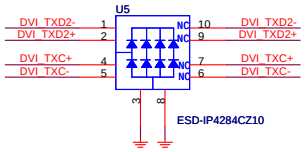
DVI level shifter

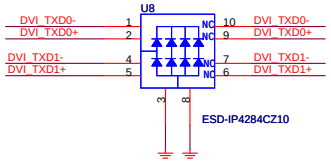
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

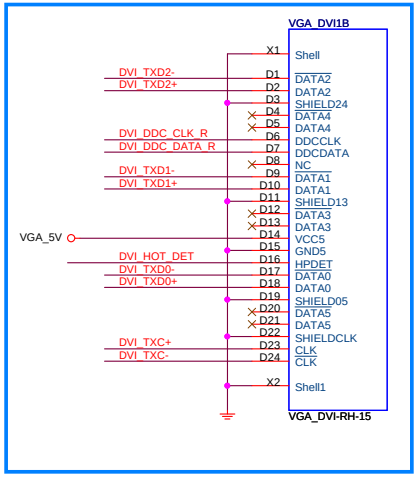


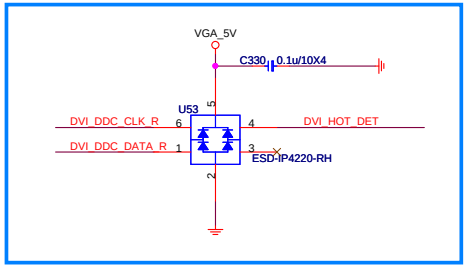


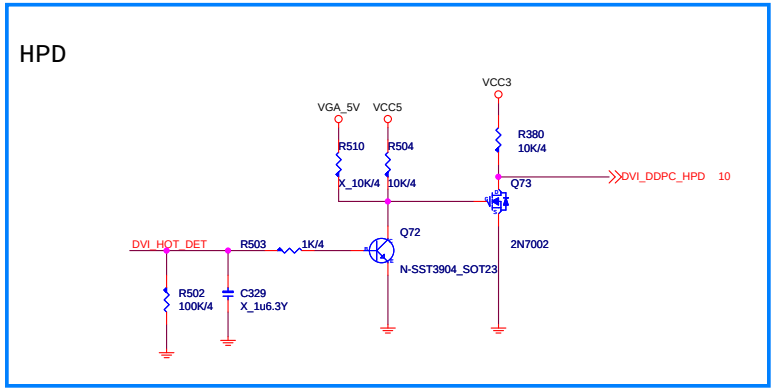


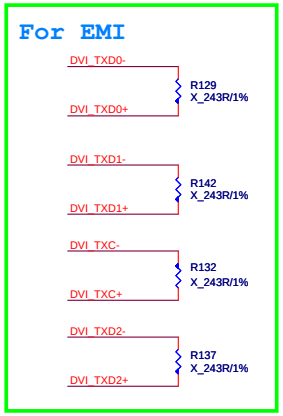


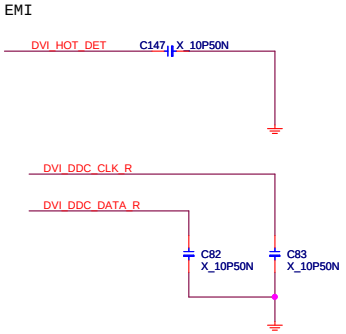












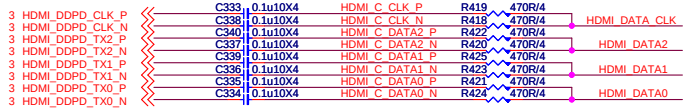
MICRO-STAR INT'L CO.,LTD

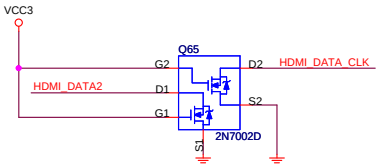
MS-7817

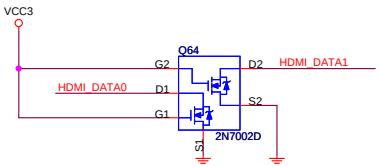
Size	Document Description	Rev
Custom	DVI transfer	30

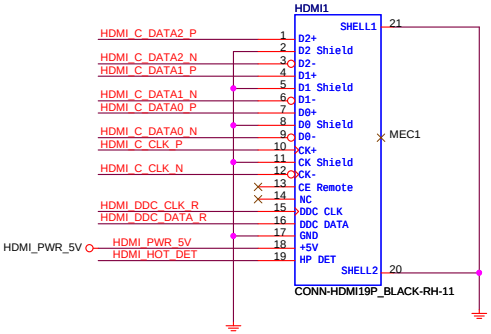
Date: Monday, October 07, 2013 Sheet 23 of 36

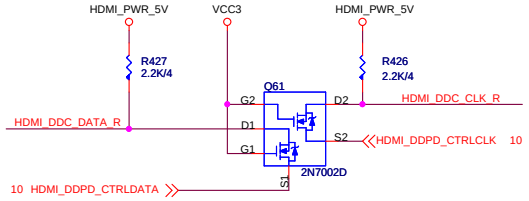
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)

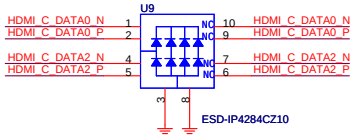


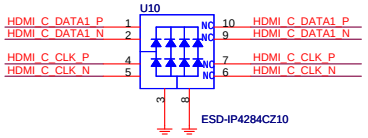


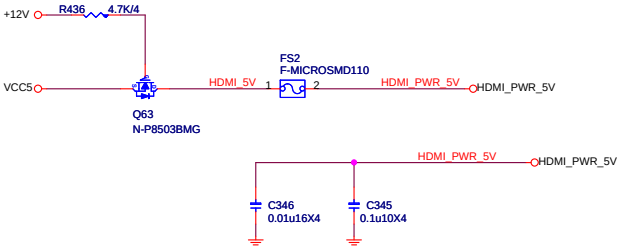


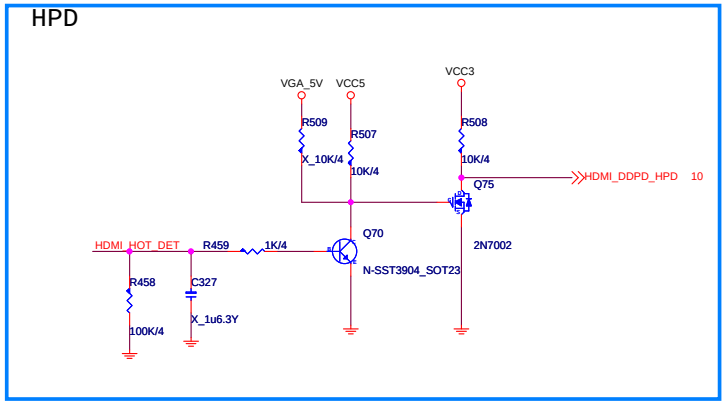


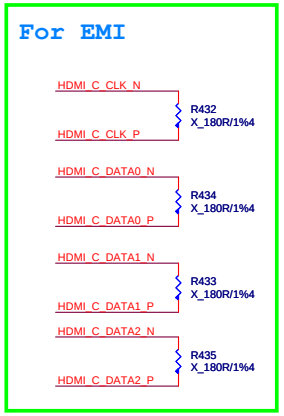


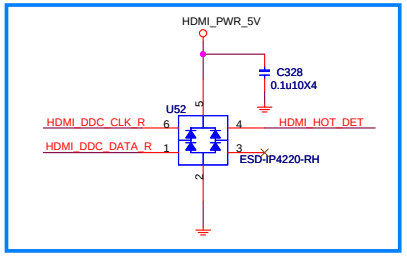










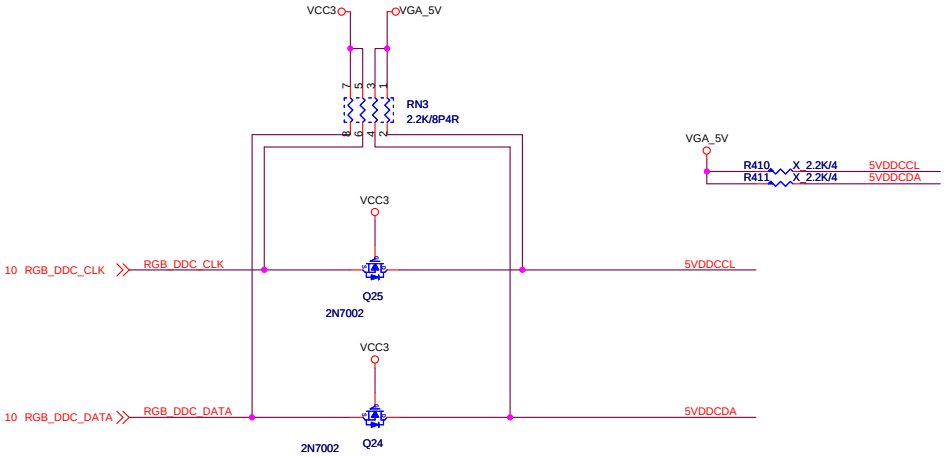


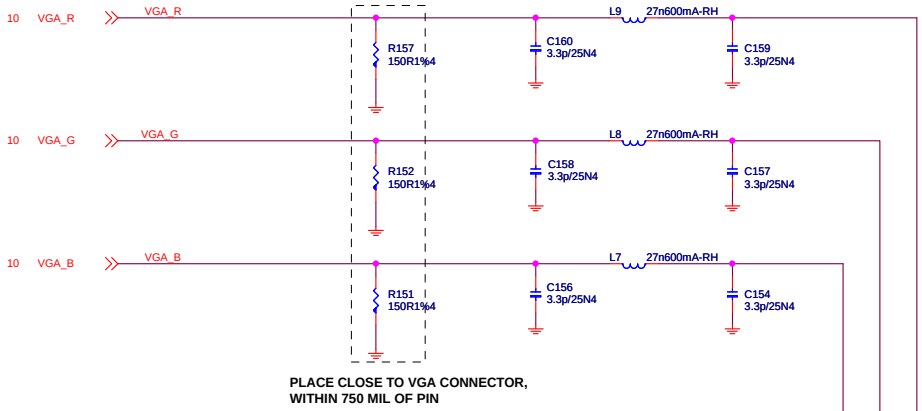
EMI

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7817	
Size: Custom	Document Description: HDMI Connector	Rev: 30
Date: Wednesday, September 18, 2013	Sheet 24 of 36	

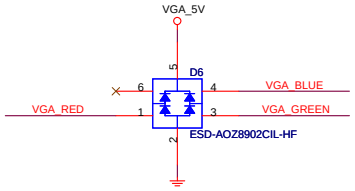
D-Sub

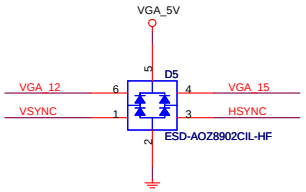
Level shift

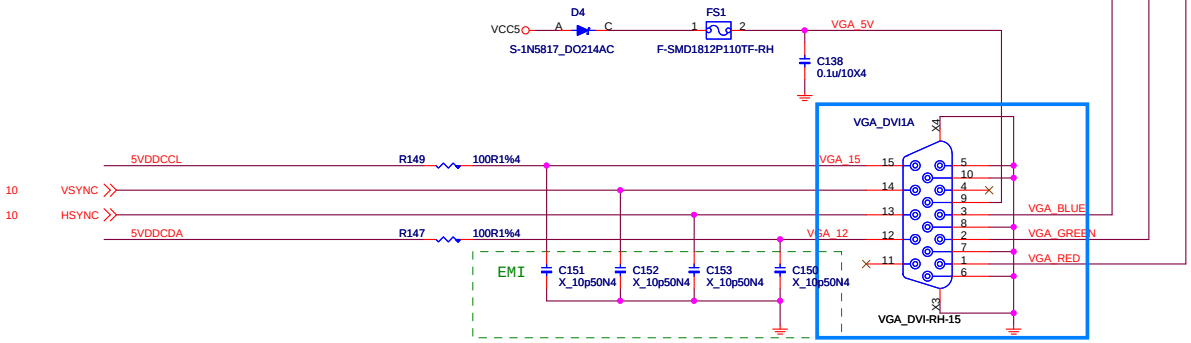




PLACE CLOSE TO VGA CONNECTOR, WITHIN 750 MIL OF PIN

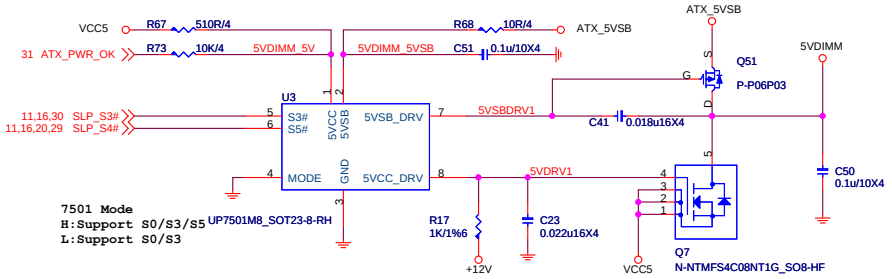




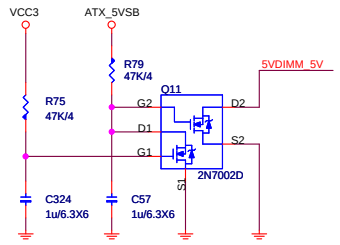


MICRO-STAR INT'L CO.,LTD		
MS-7817		
Size: Custom	Document Description: VGA Connector	Rev: 30
Date: Monday, October 07, 2013	Sheet 25 of 36	

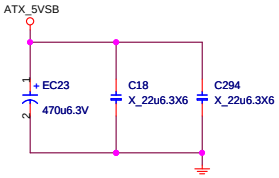
5VDIMM FOR DDR

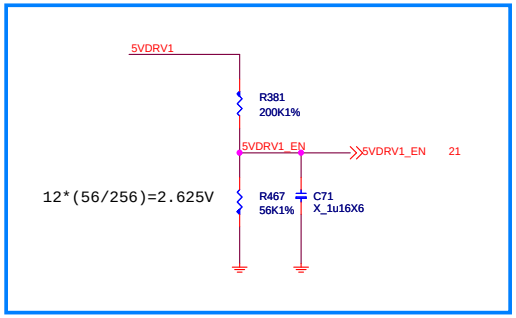


For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.



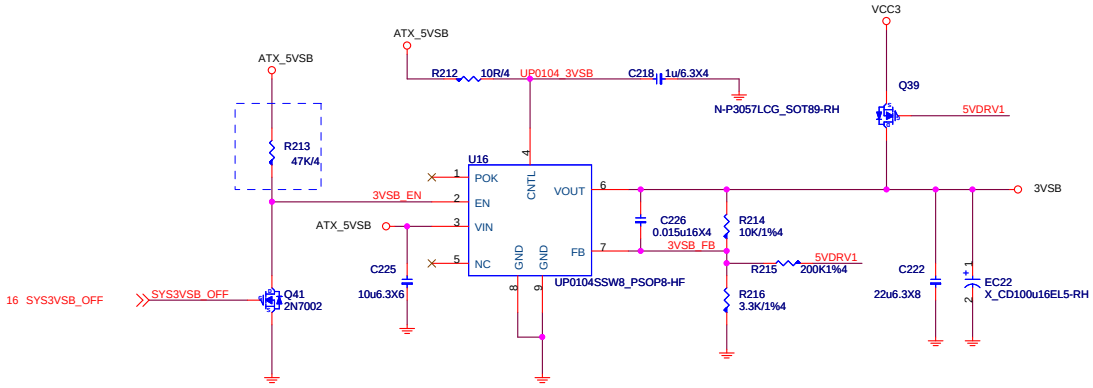
Patch coolermaster 700w power sequence





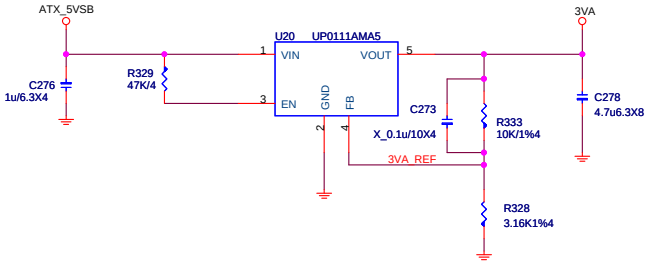
3VSB

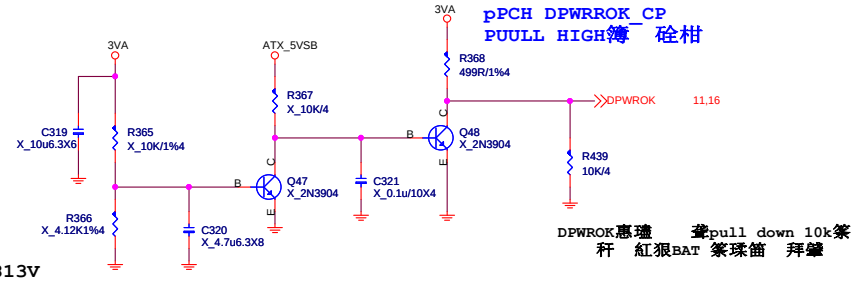
3VSB supply to PCH and other device.
Turn off when Deep S3/S5 by 5VSB off.



3VA

20mA



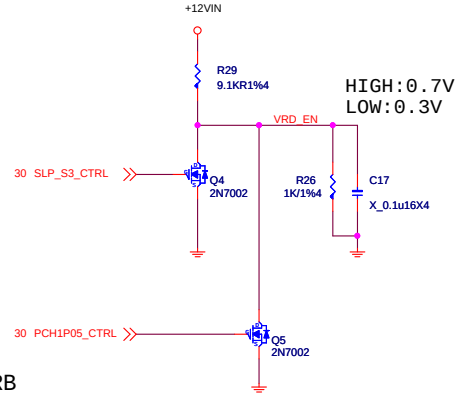


3.389Vだ溃=0.813V
2.71Vだ溃=0.65V

FOR DPWROK蛤3VA POWER
DOWN (S5-->G3)

MICRO-STAR INT'L CO.,LTD		
MS-7817		
Size: Custom	Document Description: ACPI controller UPI	Rev: 30
Date: Wednesday, October 09, 2013	Sheet 26 of 36	

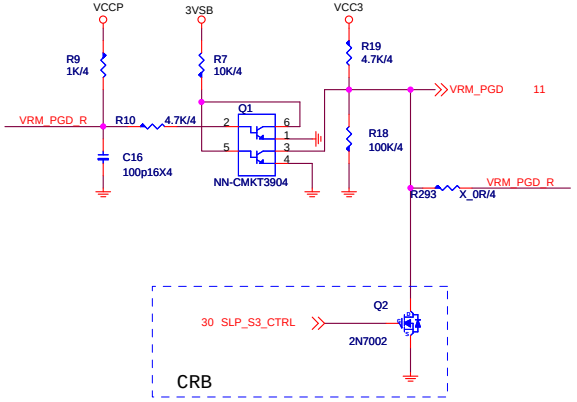
VCORE power on by s3 and 12v

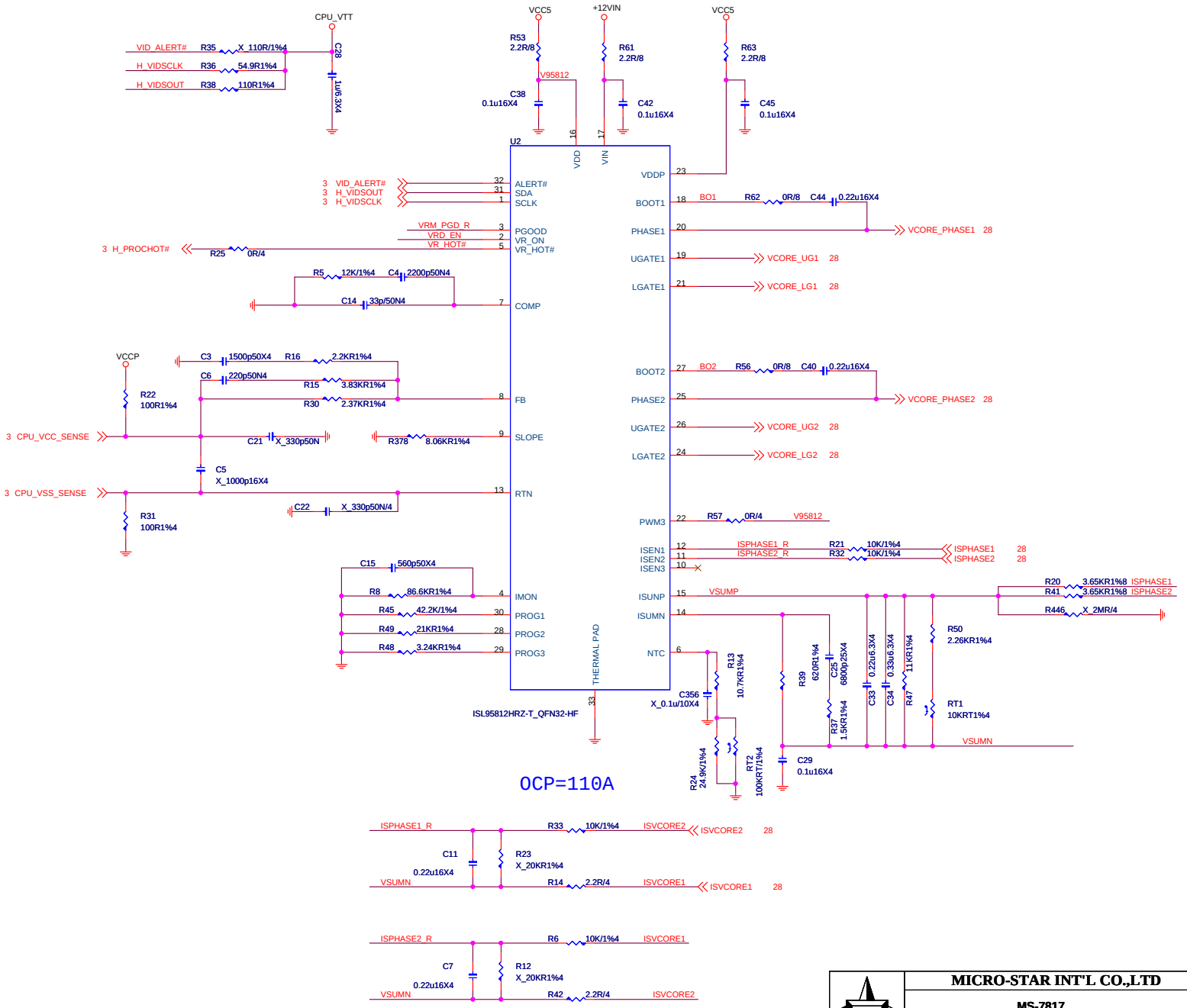


CRB

HIGH:by PCH_1P05V
LOW:by S3

VRMPWRGD LEVEL SHIFT

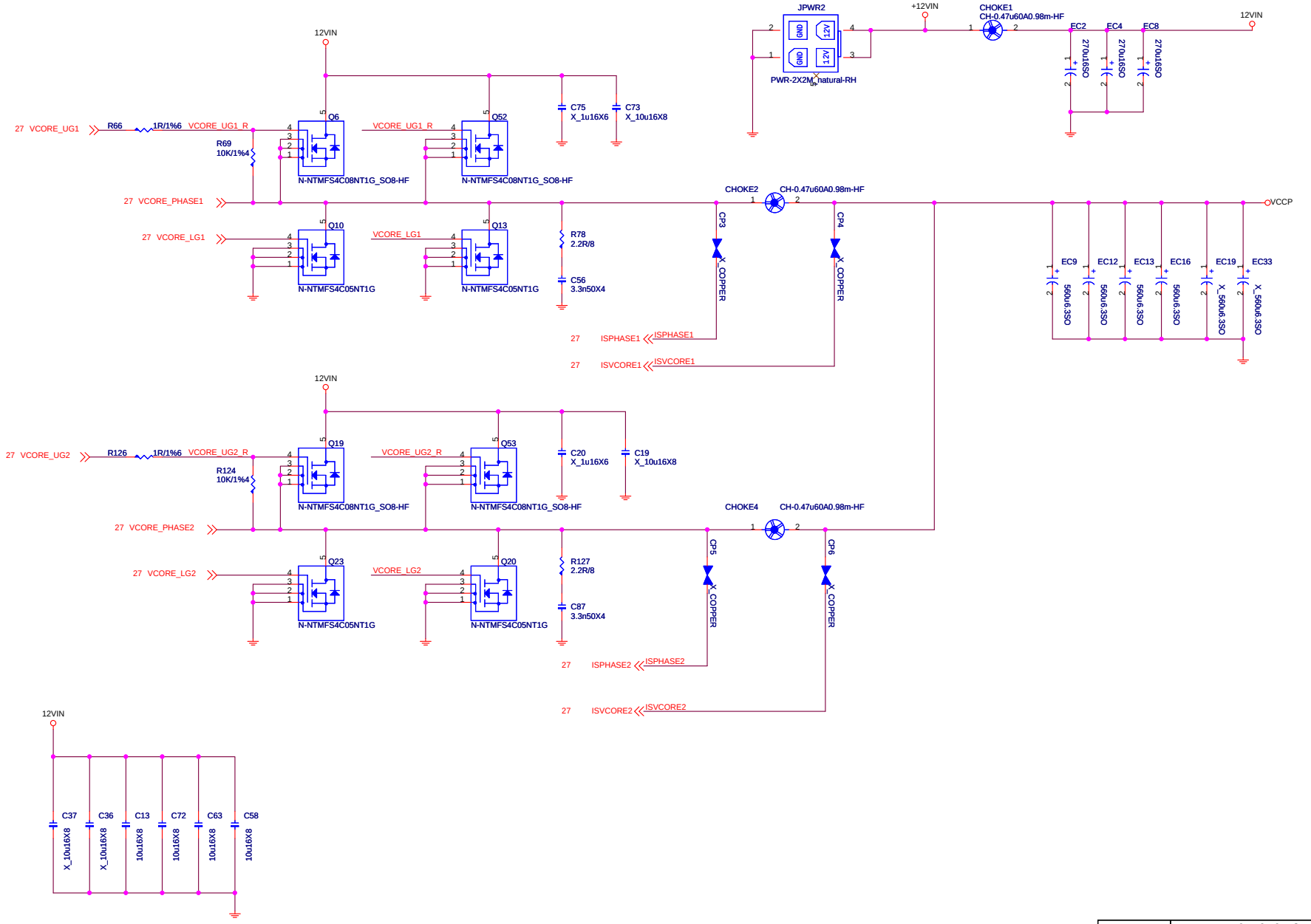




MICRO-STAR INT'L CO.,LTD		
MS-7817		
Size: Custom	Document Description: VRD12.5 - ISL95818	Rev: 30
Date: Wednesday, October 09, 2013	Sheet 27 of 36	

VCCP POWER

VCORE ICC MAX70A ICCTDC:47A 65W
LL:2.5m ohm



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7817	
Size: Custom	Document Description: VCCP POWER	Rev: 30
Date: Monday, September 23, 2013	Sheet 28 of 36	

DDR Power:1.5V

DDR3_1.5V 4.2A+6A+0.5A+5.921=16.621A

OCP:25A

4.2A FOR CPU

6A FOR 2DIMM

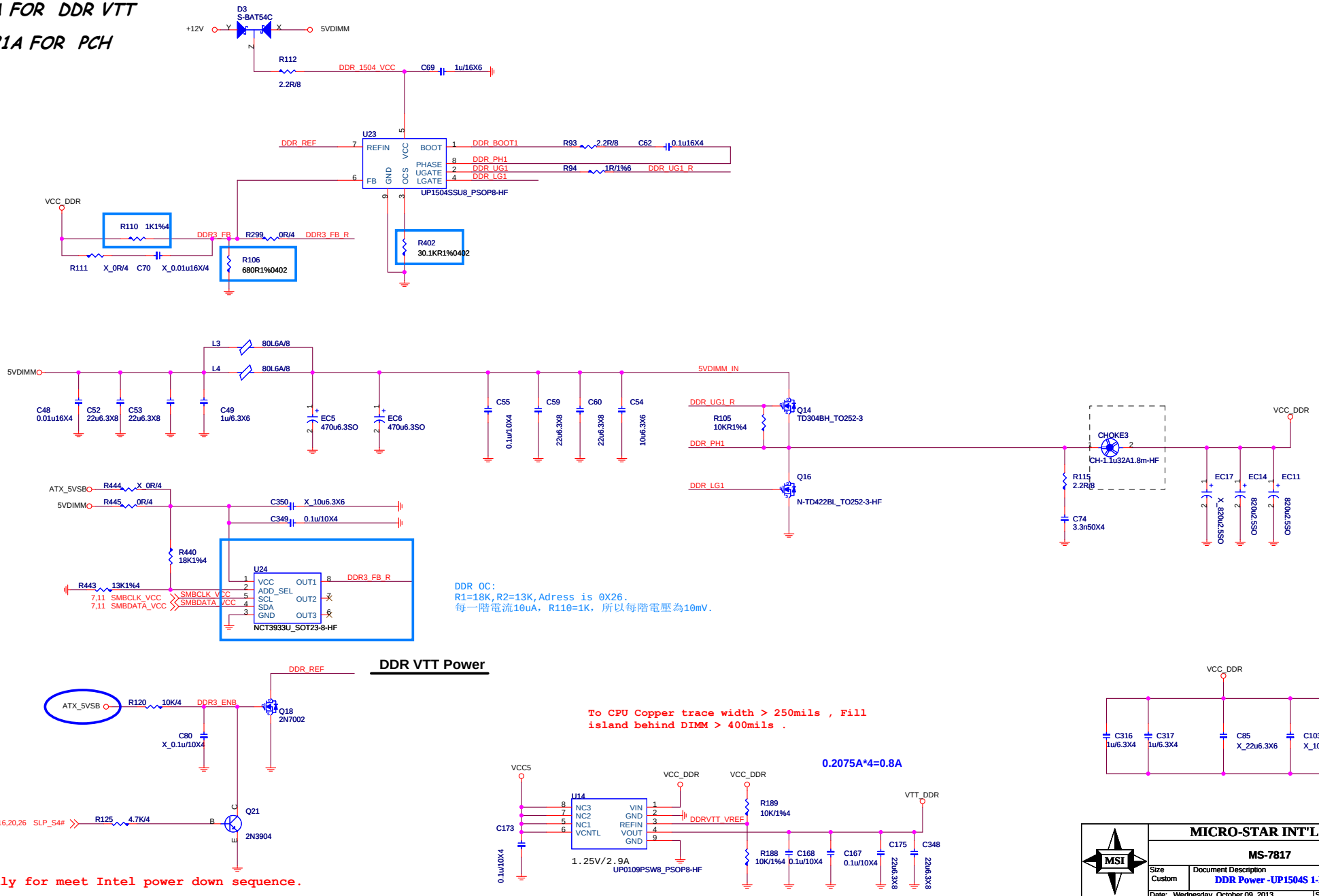
0.5A FOR DDR VTT

5.921A FOR PCH

*OCP:16.621*1.5=25A*

*OCPXRdson(Low side)=(40uA*Rocs(R402)-0.4V)*

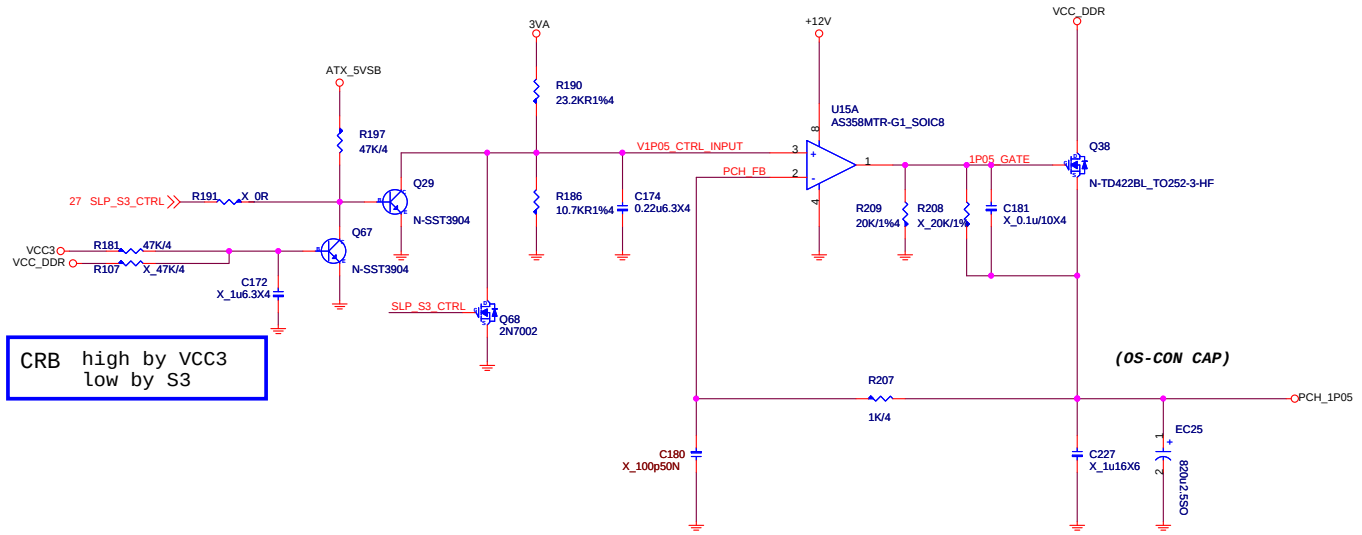
Rocs(R402)=30K



P.S. Only for meet Intel power down sequence.

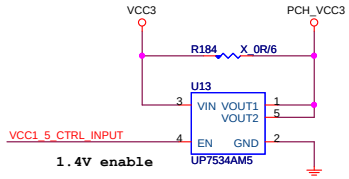
MICRO-STAR INT'L CO.,LTD	
MS-7817	
Size: Custom	Document Description: DDR Power -UP1504S 1-Phase
Rev: 30	
Date: Wednesday, October 09, 2013	Sheet 29 of 36

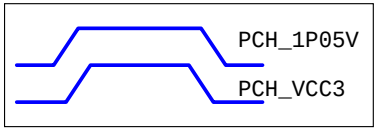
PCH Power:1.05V 5.747A



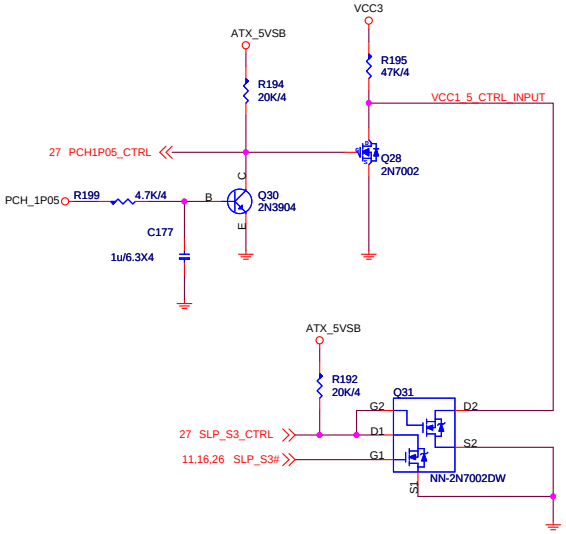
CRB high by VCC3
low by S3

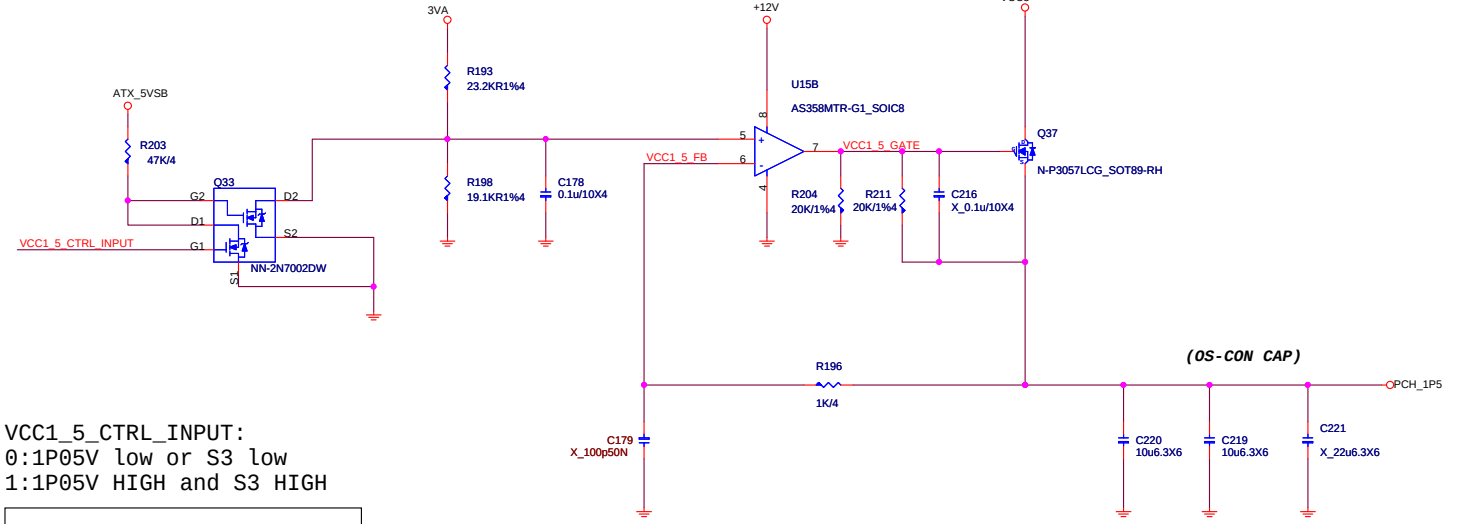
0.133A



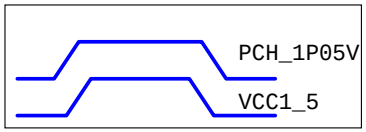


PCH Power:1.5V 0.183A



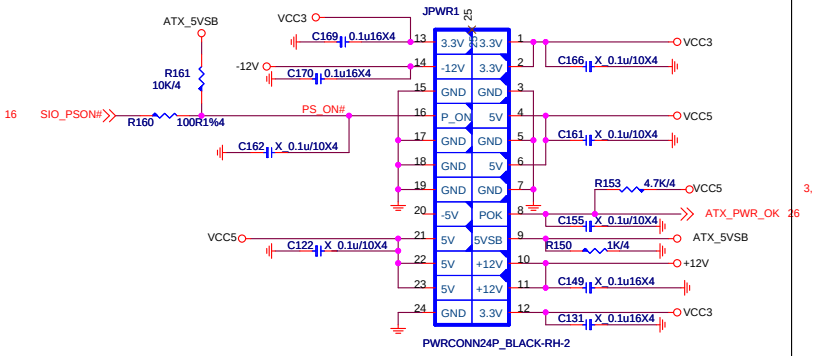


VCC1_5_CTRL_INPUT:
0:1P05V low or S3 low
1:1P05V HIGH and S3 HIGH



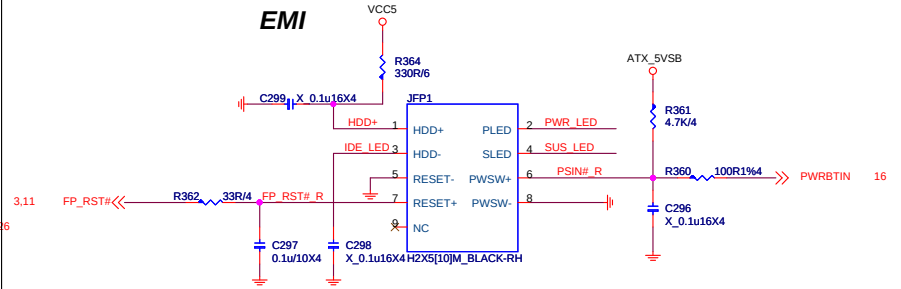
MICRO-STAR INT'L CO.,LTD		
MS-7817		
Size: Custom	Document Description: PCH Power - OP+MOS	Rev: 30
Date: Wednesday, October 09, 2013	Sheet 30 of 36	

ATX POWER CONNECTOR

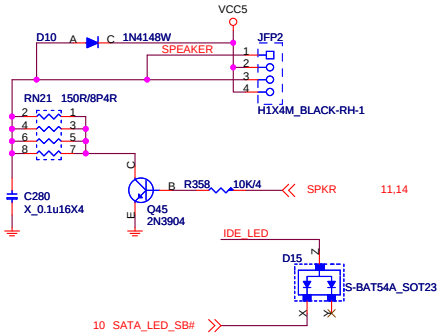


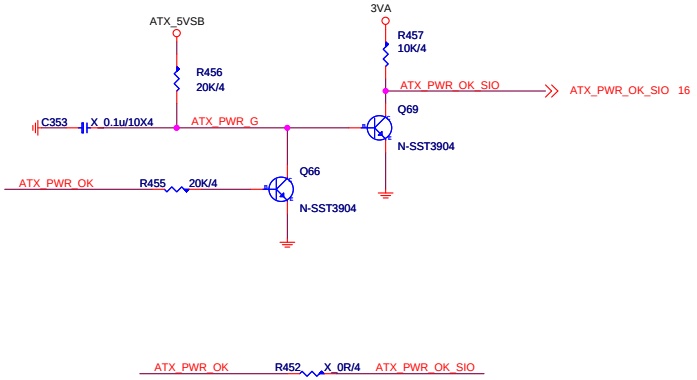
FRONT PANNEL

EMI

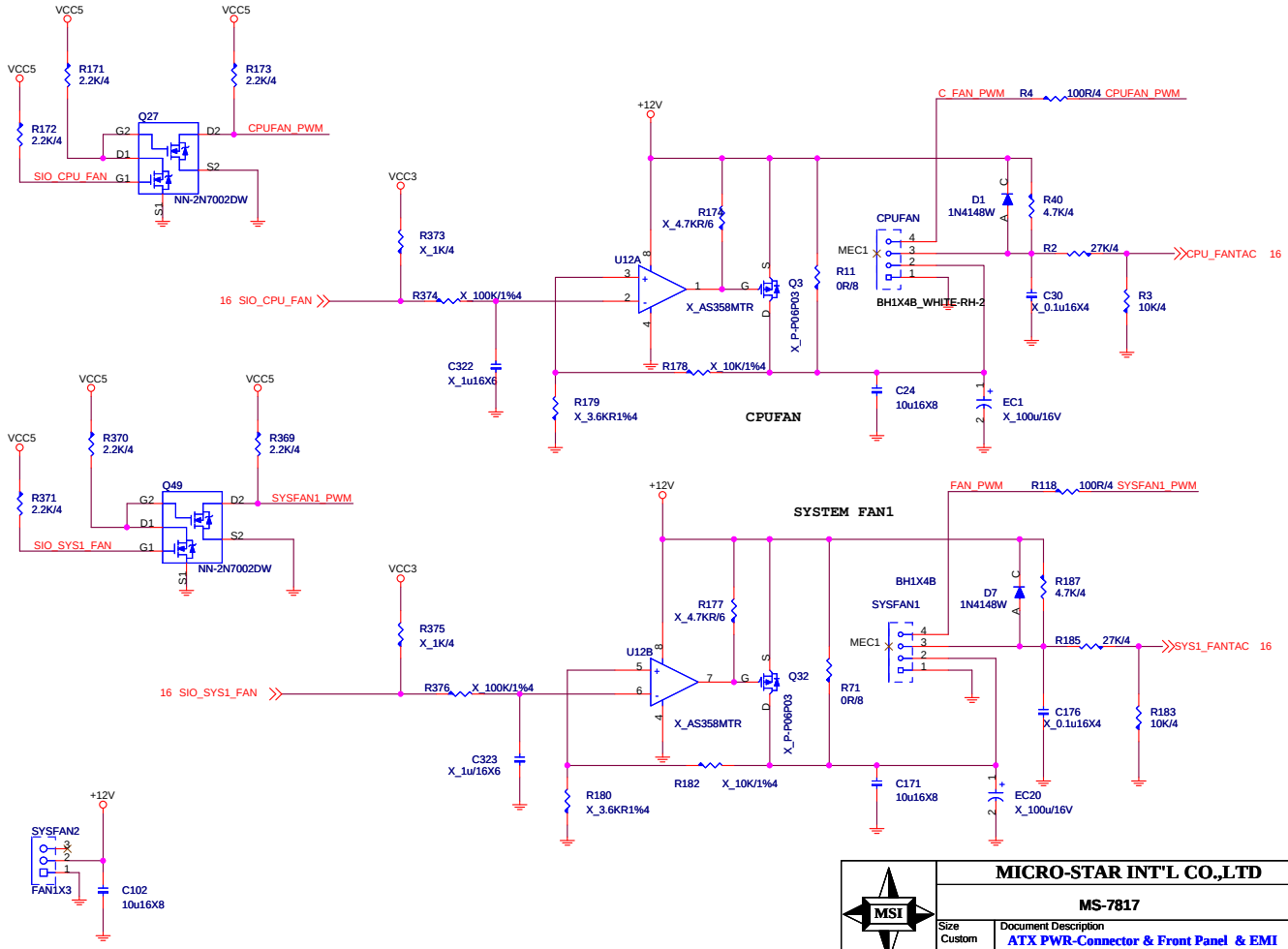


Speaker Pin Header

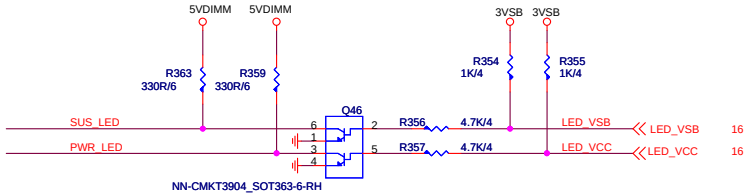




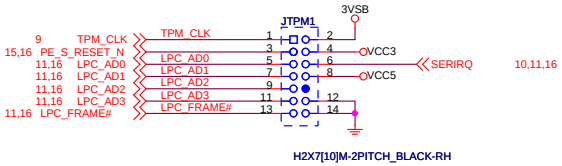
FAN-COUNTROL CIRCUIT



LED (for NV5533)



TPM/JLPC



MICRO-STAR INT'L CO.,LTD	
MS-7817	
Size: Custom	Document Description: ATX PWR-Connector & Front Panel & EMI
Rev: 30	
Date: Wednesday, October 09, 2013	Sheet 31 of 36

MARKET Name

LABEL1

LABEL

HDMI

LABEL3

LABEL

LABEL4

X_LABEL

Battery

BAT1_X1

BAT-BCR2032P-RH

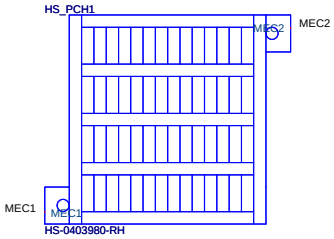
CPU Socket

CPU_H1

CPU_H1

PCH Heatsink

HS_PCH1



HS-0403980-RH

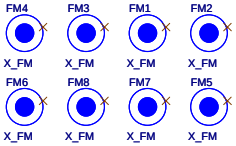
PCB1

7817_30

P/N:PK0-0781730-G37/PK0-0781730-E48

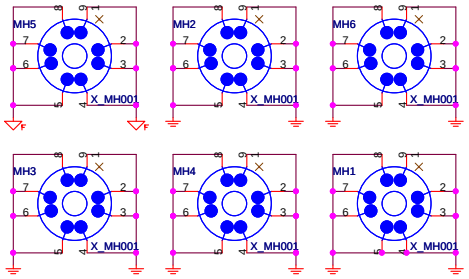
VCCP — VCCP
VCC_DDR — VCC_DDR
VTT_DDR — VTT_DDR
PCH_1P05 — PCH_1P05
PCH_1P5 — PCH_1P5
5VDIMM — 5VDIMM
3VSB — 3VSB
PCH_VCC3 — PCH_VCC3
3VA — 3VA

Optical Fiducial Marks-120



Simulation

Mounting Holes



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	MS-7817	
Size: Custom	Document Description: Manual Parts	Rev: 30
Date: Wednesday, October 09, 2013	Sheet 32 of 36	